54/74 Family
SSI Circuits

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54H SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−500			−100			−400			−1000	μA
	74 Family			−400			−500			−200			−400			−1000	
Low-level output current, I_{OL}	54 Family			16			20			2			4			20	mA
	74 Family			16			20			3.6			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54H SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.8			0.7			0.7			0.8	V
					74 Family			0.8			0.8			0.7			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §					−1.5			−1.5						−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, I_{OH} = MAX	V_{IL} = V_{IL} max,	54 Family	2.4	3.4		2.4	3.5		2.4	3.3		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.4	3.5		2.4	3.2		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.2	0.4		0.25	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS												0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			1			0.1						1	mA
					V_I = 7 V												0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			50			10							μA
					V_{IH} = 2.7 V												20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.3 V									−0.18							mA
					V_{IL} = 0.4 V			−1.6			−2						−0.4				
					V_{IL} = 0.5 V															−2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		54 Family	−20		−55	−40		−100	−3		−15	−20		−100	−40		−100	mA
					74 Family	−18		−55	−40		−100	−3		−15	−20		−100	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page															mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
♦Not more than one output should be shorted at a time, and for SN54H'/SN74H', SN54LS'/SN74LS', and SN54S'/SN74S', duration of short-circuit should not exceed 1 second.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'00	4	8	12	22	2
'04	6	12	18	33	2
'10	3	6	9	16.5	2
'20	2	4	6	11	2
'30	1	2	3	6	2
'H00	10	16.8	26	40	4.5
'H04	16	26	40	58	4.5
'H10	7.5	12.6	19.5	30	4.5
'H20	5	8.4	13	20	4.5
'H30	2.5	4.2	6.5	10	4.5
'L00	0.44	0.8	1.16	2.04	0.20
'L04	0.66	1.2	1.74	3.06	0.20
'L10	0.33	0.6	0.87	1.53	0.20
'L20	0.22	0.4	0.58	1.02	0.20
SN54L30	0.11	0.33	0.29	0.51	0.20
SN74L30	0.11	0.2	0.29	0.51	0.20
'LS00	0.8	1.6	2.4	4.4	0.4
'LS04	1.2	2.4	3.6	6.6	0.4
'LS10	0.6	1.2	1.8	3.3	0.4
'LS20	0.4	0.8	1.2	2.2	0.4
'LS30	0.35	0.5	0.6	1.1	0.48
'S00	10	16	20	36	3.75
'S04	15	24	30	54	3.75
'S10	7.5	12	15	27	3.75
'S20	5	8	10	18	3.75
'S30	3	5	5.5	10	4.25
'S133	3	5	5.5	10	4.25

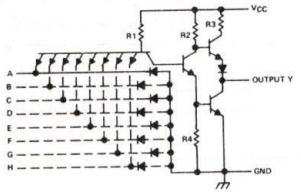
switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'00, '10	C_L = 15 pF, R_L = 400 Ω		11	22		7	15
'04, '20			12	22		8	15
'30			13	22		8	15
'H00	C_L = 25 pF, R_L = 280 Ω		5.9	10		6.2	10
'H04			6	10		6.5	10
'H10			5.9	10		6.3	10
'H20			6	10		7	10
'H30			6.8	10		8.9	12
'L00, 'L04, 'L10, L20	C_L = 50 pF, R_L = 4 kΩ		35	60		31	60
'L30			35	60		70	100
'LS00, 'LS04 'LS10, 'LS20	C_L = 15 pF, R_L = 2 kΩ		9	15		10	15
'LS30			8	15		13	20
'S00, 'S04	C_L = 15 pF, R_L = 280 Ω		3	4.5		3	5
'S10, 'S20	C_L = 50 pF, R_L = 280 Ω		4.5			5	
'S30, 'S133	C_L = 15 pF, R_L = 280 Ω		4	6		4.5	7
	C_L = 50 pF, R_L = 280 Ω		5.5			6.5	

#Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

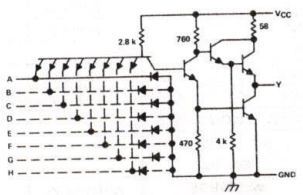
schematics (each gate)



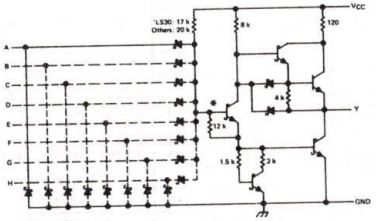
CIRCUIT	R1	R2	R3	R4
'00, '04, '10, '20, '30	4 k	1.6 k	130	1 k
'L00, 'L04, 'L10, 'L20, 'L30	40 k	20 k	500	12 k

'00, '04, '10, '20, '30
'L00, 'L04, 'L10, 'L20, 'L30, CIRCUITS

Input clamp diodes not on SN54L'/SN74L' circuits.

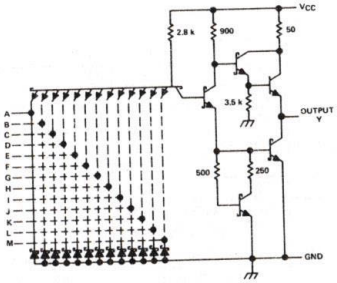


'H00, 'H04, 'H10, 'H20, 'H30 CIRCUITS



'LS00, 'LS04, 'LS10, 'LS20, 'LS30 CIRCUITS

*The 12-kΩ resistor is not on 'LS30.



'S00, 'S04, 'S10, 'S20, 'S30, 'S133 CIRCUITS

Resistor values shown are nominal and in ohms.

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recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '01, '03, '05, '12, '22			SERIES 54H SERIES 74H 'H01, 'H05, 'H22			SERIES 54L SERIES 74L 'L01, 'L03			SERIES 54LS SERIES 74LS 'LS01, 'LS03, 'LS05, 'LS12, 'LS22			SERIES 54S SERIES 74S 'S03, 'S05, 'S22			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family		4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family		4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}					5.5			5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}	54 Family				16			20			2			4			20	mA
	74 Family				16			20			3.6			8			20	
Operating free-air temperature, T_A	54 Family		−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family		0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '01, '03, '05, '12, '22			SERIES 54H SERIES 74H 'H01, 'H05, 'H22			SERIES 54L SERIES 74L 'L01, 'L03			SERIES 54LS SERIES 74LS 'LS01, 'LS03, 'LS05, 'LS12, 'LS22			SERIES 54S SERIES 74S 'S03, 'S05, 'S22			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.8			0.6			0.7			0.8	V
					74 Family			0.8			0.8			0.6			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §					−1.5			−1.5						−1.5			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IL} = V_{IL} max, V_{OH} = 5.5 V					250			250			50			100			250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS											0.25	0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			1			0.1						1	mA
					V_I = 7 V												0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			50			10							μA
					V_{IH} = 2.7 V												20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.3 V									−0.18							mA
					V_{IL} = 0.4 V			−1.6			−2						−0.4				
					V_{IL} = 0.5 V															−2	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page															mA

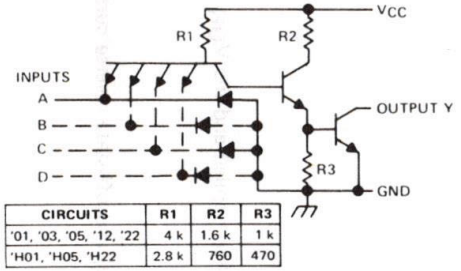
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per Gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'01	4	8	12	22	2
'03	4	8	12	22	2
'05	6	12	18	33	2
'12	3	6	9	16.5	2
'22	2	4	6	11	2
'H01	10	16.8	26	40	4.1
'H05	16	26	40	58	4.67
'H22	5	8.4	13	20	4.1
'L01	0.44	0.8	1.16	2.04	0.20
'L03	0.44	0.8	1.16	2.04	0.20
'LS01	0.8	1.6	2.4	4.4	0.4
'LS03	0.8	1.6	2.4	4.4	0.4
'LS05	1.2	2.4	3.6	6.6	0.4
'LS12	0.7	1.4	1.8	3.3	0.42
'LS22	0.4	0.8	1.2	2.2	0.4
'S03	6	13.2	20	36	3.25
'S05	9	19.8	30	54	3.25
'S22	3	6.6	10	18	3.25

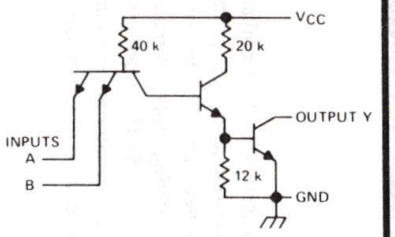
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)

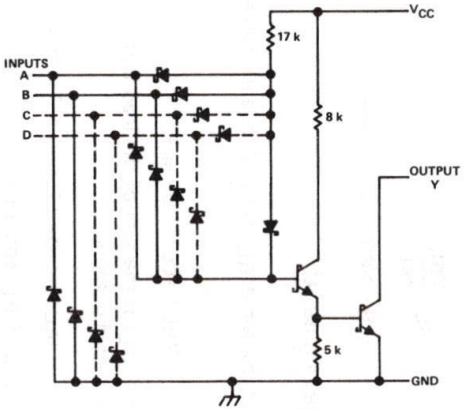


CIRCUITS	R1	R2	R3
'01, '03, '05, '12, '22	4 k	1.6 k	1 k
'H01, 'H05, 'H22	2.8 k	760	470

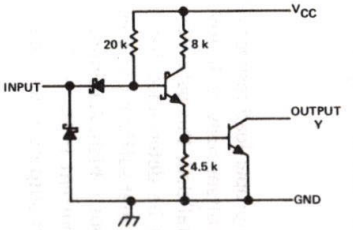
'01, '03, '05, '12, '22, 'H01, 'H05, 'H22 CIRCUITS



'L01, 'L03 CIRCUITS



'LS01, 'LS03, 'LS12, 'LS22 CIRCUITS

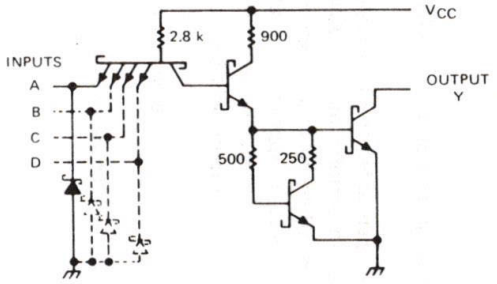


'LS05 CIRCUITS

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'01, '03	C_L = 15 pF, R_L = 4 kΩ for t_{PLH}, 400 Ω for t_{PHL}		35	45		8	15
'05			40	55		8	15
'12, '22			35	45		8	15
'H01, 'H05, 'H22	C_L = 25 pF, R_L = 280 Ω		10	15		7.5	12
'L01, 'L03	C_L = 50 pF, R_L = 4 kΩ		60	90		33	60
'LS01, 'LS03, 'LS05, 'LS12, 'LS22	C_L = 15 pF, R_L = 2 kΩ		17	32		15	28
'S03, 'S05, 'S22	C_L = 15 pF, R_L = 280 Ω	2	5	7.5	2	4.5	7
	C_L = 50 pF, R_L = 280 Ω		7.5			7	

#Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.



'S03, 'S05, 'S22 CIRCUITS

Resistor values shown are nominal and in ohms.

OPEN-COLLECTOR OUTPUT APPLICATION DATA

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine standard loads of its own series. When no other open-collector gates are paralleled, this gate may be used to drive ten loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if only one of the paralleled outputs is sinking all the currents.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH\ min}$$

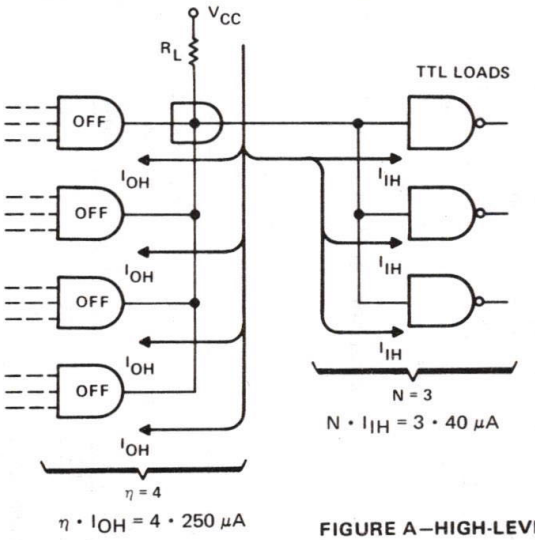
The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of standard loads.



Calculation:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.001 + 0.00012}\ \Omega = \frac{2.6}{0.00112}\ \Omega = 2321\ \Omega$$

Values shown are for Series 54/74 standard inputs and outputs. For devices in other series, substitute appropriate values.

FIGURE A—HIGH-LEVEL CIRCUIT CONDITIONS

6

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APPLICATION DATA

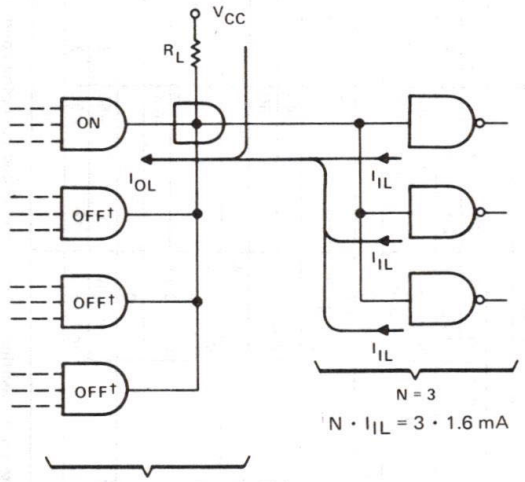
low-level (on-state) circuit calculations (see figure B)

The current through the resistor must be limited to the maximum sink current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to the recommended maximum I_{OL}, the maximum current which will ensure that the low-level output voltage, V_{OL}, will be below V_{OL} max.

Also, fan-out must be considered. Part of I_{OL} will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048}\ \Omega = \frac{4.6}{0.0112}\ \Omega = 410\ \Omega$$

Values shown are for Series 54/74 standard inputs and outputs. For devices in other series, substitute the appropriate values.

†Current into OFF outputs is negligible at the low logic level.

FIGURE B–LOW-LEVEL CIRCUIT CONDITIONS

6

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '02			SERIES 54 / SERIES 74 '25, '27			SERIES 54L / SERIES 74L 'L02			SERIES 54LS / SERIES 74LS 'LS02, 'LS27			SERIES 54S / SERIES 74S 'S02, 'S260			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−800			−100			−400			−1000	μA
	74 Family			−400			−800			−200			−400			−1000	
Low-level output current, I_{OL}	54 Family			16			16			2			4			20	mA
	74 Family			16			16			3.6			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†			SERIES 54 / SERIES 74 '02, '25, '27			SERIES 54L / SERIES 74L 'L02			SERIES 54LS / SERIES 74LS 'LS02 'LS27			SERIES 54S / SERIES 74S 'S02, 'S260			UNIT
							MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		1, 2				2			2			2			2			V
V_{IL}	Low-level input voltage		1, 2			54 Family			0.8			0.7			0.7			0.8	V
						74 Family			0.8			0.7			0.8			0.8	
V_{IK}	Input clamp voltage		3	V_{CC} = MIN, I_I = §					−1.5						−1.5			−1.2	V
V_{OH}	High-level output voltage		1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX		54 Family	2.4	3.4		2.4	3.3		2.5	3.4		2.5	3.4		V
						74 Family	2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
						74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
					I_{OL} = 4 mA	Series 74LS								0.25	0.4				
I_I	Input current at maximum input voltage		4	V_{CC} = MAX		V_I = 5.5 V			1			0.1						1	mA
						V_I = 7 V									0.1				
I_{IH}	High-level input current	Data inputs	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			10							μA
		Strobe of '25							160										
		All inputs				V_{IH} = 2.7 V									20			50	
I_{IL}	Low-level input current	All inputs	5	V_{CC} = MAX		V_{IL} = 0.3 V					−0.18								mA
		Data inputs				V_{IL} = 0.4 V			−1.6						−0.4				
		Strobe of '25							−6.4										
		All inputs				V_{IL} = 0.5 V												−2	
I_{OS}	Short-circuit output current♦		6	V_{CC} = MAX		54 Family	−20		−55	−3		−15	−20		−100	−40		−100	mA
						74 Family	−18		−55	−3		−15	−20		−100	−40		−100	
I_{CC}	Supply current		7	V_{CC} = MAX			See table on next page												mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS' and SN54S/SN74S'.

♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of output short-circuit should not exceed one second.

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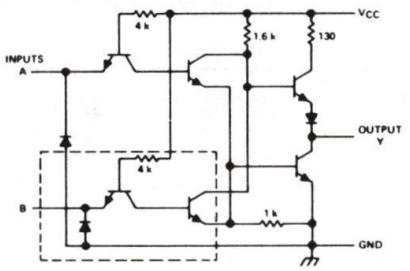
supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'02	8	16	14	27	2.75
'25	8	16	10	19	2.25
'27	10	16	16	26	4.34
'L02	0.8	1.6	1.4	2.6	0.275
'LS02	1.6	3.2	2.8	5.4	0.55
'LS27	2.0	4	3.4	6.8	0.9
'S02	17	29	26	45	5.38
'S260	17	29	26	45	10.75

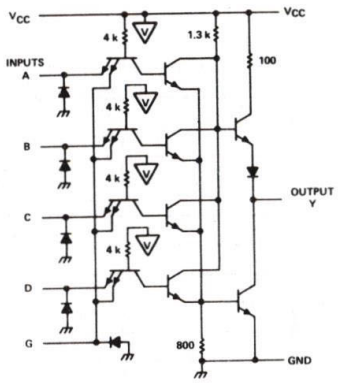
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)



The portion of the schematic within the dashed lines is repeated for the C input of the '27.

'02, '27 CIRCUITS



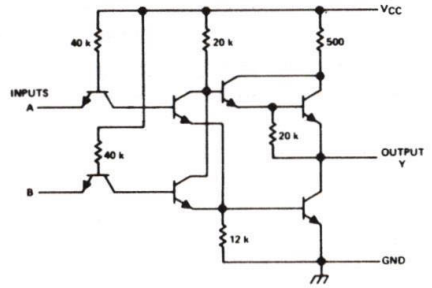
'25 CIRCUITS

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'02	C_L = 15 pF, R_L = 400 Ω		12	22		8	15
'25			13	22		8	15
'27			10	15		7	11
'L02	C_L = 50 pF, R_L = 4 kΩ		31	60		35	60
'LS02, 'LS27	C_L = 15 pF, R_L = 2 kΩ		10	15		10	15
'S02	C_L = 15 pF, R_L = 280 Ω		3.5	5.5		3.5	5.5
	C_L = 50 pF, R_L = 280 Ω		5			5	
'S260	C_L = 15 pF, R_L = 280 Ω		4	5.5		4	6

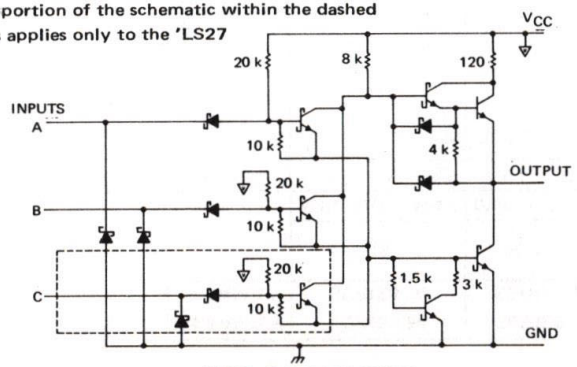
#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

Resistor values are nominal and in ohms.

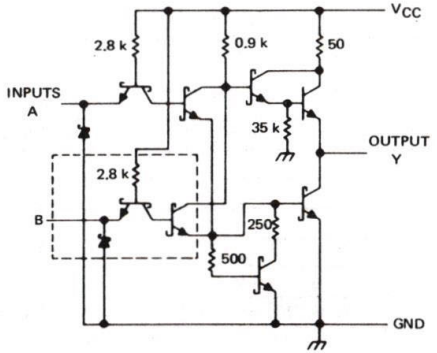


'L02 CIRCUITS

The portion of the schematic within the dashed lines applies only to the 'LS27



'LS02, 'LS27 CIRCUITS



The portion of the schematic within the dashed lines is repeated for each additional input of the 'S260, and the 0.9-kΩ resistor is changed to 0.6 kΩ.

'S02, 'S260 CIRCUITS

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '08,			SERIES 54H SERIES 74H 'H11, 'H21			SERIES 54LS SERIES 74LS 'LS08, 'LS11, 'LS21			SERIES 54S SERIES 74S 'S08, 'S11			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−800			−500			−400			−1000	μA
Low-level output current, I_{OL}		54 Family			16			20			4			20	mA
		74 Family			16			20			8			20	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	−55		125	−55		125	°C
		74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '08			SERIES 54H SERIES 74H 'H11, 'H21			SERIES 54LS SERIES 74LS 'LS08, 'LS11, 'LS21			SERIES 54S SERIES 74S 'S08, 'S11			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §					−1.5			−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	54 Family	2.4	3.4		2.4	3.4		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN,	I_{OL} = MAX	54 Family		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			V_{IH} = 2 V	I_{OL} = 4 mA	Series 74LS								0.25	0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			1						1	mA
					V_I = 7 V									0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			50							μA
					V_{IH} = 2.7 V									20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			−1.6			−2			−0.4				mA
					V_{IL} = 0.5 V												−2	
I_{OS}	Short circuit output current♦	6	V_{CC} = MAX		54 Family	−20		−55	−40		−100	−20		−100	−40		−100	mA
					74 Family	−18		−55	−40		−100	−20		−100	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page												mA

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡All typical values are at V_{CC} = 25°C.

§I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.

♦Not more than one output should be shorted at a time, and for SN54H'/SN74H', SN54LS'/SN74LS' and SN54S'/SN74S', duration of output short circuit should not exceed one second.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'08	11	21	20	33	3.88
'H11	18	30	30	48	8
'H21	12	20	20	32	8
'LS08	2.4	4.8	4.4	8.8	0.85
'LS11	1.8	3.6	3.3	6.6	0.85
'LS21	1.2	2.4	2.2	4.4	0.85
'S08	18	32	32	57	6.25
'S11	13.5	24	24	42	6.25

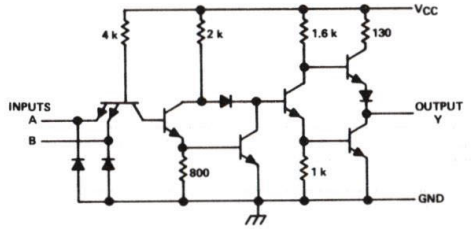
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

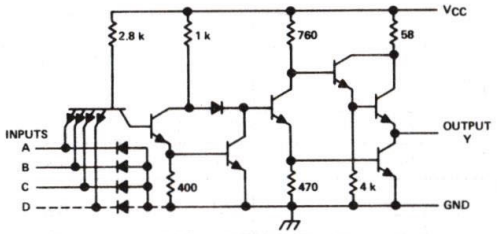
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'08	C_L = 15 pF, R_L = 400 Ω		17.5	27		12	19
'H11, 'H21	C_L = 25 pF, R_L = 280 Ω		7.6	12		8.8	12
'LS08, 'LS11 'LS21	C_L = 15 pF, R_L = 2 kΩ		8	15		10	20
'S08, 'S11	C_L = 15 pF, R_L = 280 Ω		4.5	7		5	7.5
	C_L = 50 pF, R_L = 280 Ω		6			7.5	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

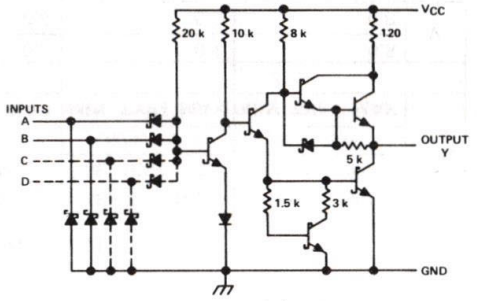
schematics (each gate)



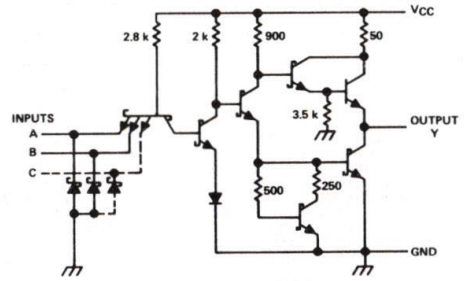
'08 CIRCUITS



'H11, 'H21 CIRCUITS



'LS08, 'LS11, 'LS21 CIRCUITS



'S08, 'S11 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '09			SERIES 54H SERIES 74H 'H15			SERIES 54LS SERIES 74LS 'LS09, 'LS15			SERIES 54S SERIES 74S 'S09, 'S15			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}	54 Family			16			20			4			20	mA
	74 Family			16			20			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '09			SERIES 54H SERIES 74H 'H15			SERIES 54LS SERIES 74LS 'LS09, 'LS15			SERIES 54S SERIES 74S 'S09, 'S15			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §					−1.5			−1.5			−1.5			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V,					250			250			100			250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS								0.25	0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			0.1						1	mA
					V_I = 7 V									0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			50							μA
					V_{IH} = 2.7 V									20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			−1.6			−2			−0.4				mA
					V_{IL} = 0.5 V												−2	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page												mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = − 12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS'.

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supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'09	11	21	20	33	3.88
'H15	15	25	30	48	7.5
'LS09	2.4	4.8	4.4	8.8	0.85
'LS15	1.8	3.6	3.3	6.6	0.85
'S09	18	32	32	57	6.25
'S15	10.5	19.5	24	42	5.75

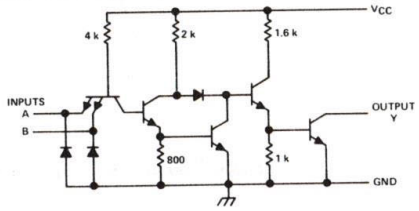
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

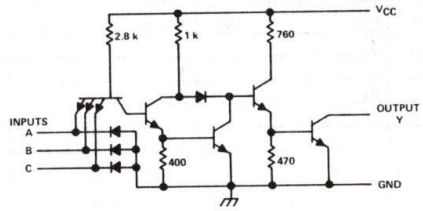
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'09	C_L = 15 pF, R_L = 400 Ω		21	32		16	24
'H15	C_L = 25 pF, R_L = 280 Ω		12	18		9	13
'LS09, 'LS15	C_L = 15 pF, R_L = 2 kΩ		20	35		17	35
'S09	C_L = 15 pF, R_L = 280 Ω		6.5	10		6.5	10
	C_L = 50 pF, R_L = 280 Ω		9			9	
'S15	C_L = 15 pF, R_L = 280 Ω		5.5	8.5		6	9
	C_L = 50 pF, R_L = 280 Ω		8.5			8	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

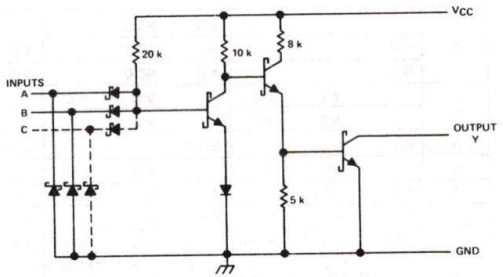
schematics (each gate)



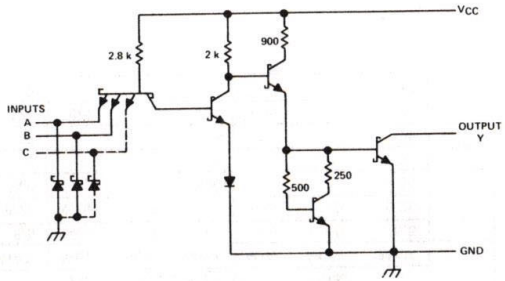
'09 CIRCUITS



'H15 CIRCUITS



'LS09, 'LS15 CIRCUITS



'S09, 'S15 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74						SERIES 54LS / SERIES 74LS			SERIES 54S / SERIES 74S			UNIT
		'13			'14, '132			'LS13, 'LS14, 'LS132			'S132			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High level output current, I_{OH}				−800			−800			−400			−1000	μA
Low-level output current, I_{OL}	54 Family			16			16			4			20	mA
	74 Family			16			16			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 / SERIES 74						SERIES 54LS / SERIES 74LS			SERIES 54S / SERIES 74S			UNIT
						'13			'14, '132			'LS13, 'LS14, 'LS132			'S132			
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage	8	V_{CC} = 5 V			1.5	1.7	2	1.5	1.7	2	1.4	1.6	1.9	1.6	1.77	1.9	V
V_{T-}	Negative-going threshold voltage	9	V_{CC} = 5 V			0.6	0.9	1.1	0.6	0.9	1.1	0.5	0.8	1	1.1	1.22	1.4	V
	Hysteresis (V_{T+}-V_{T-})	8, 9	V_{CC} = 5 V			0.4	0.8		0.4	0.8		0.4	0.8		0.2	0.55		V
V_{IK}	Input clamp voltage	3	V_{CC} = MIN,	I_I = §				−1.5			−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	9	V_{CC} = MIN, V_I = V_{T-} min	I_{OH} = MAX,	54 Family	2.4	3.4		2.4	3.4		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	8	V_{CC} = MIN, V_I = V_{T+} max	I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS								0.25	0.4				
I_{T+}	Input current at positive-going threshold	8	V_{CC} = 5 V,	V_I = V_{T+}			−0.65			−0.43			−0.14			−0.9		mA
I_{T-}	Input current at negative-going threshold	9	V_{CC} = 5 V,	V_I = V_{T-}			−0.85			−0.56			−0.18			−1.1		mA
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			1						1	mA
					V_I = 7 V									0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_I = 2.4 V			40			40							μA
					V_I = 2.7 V									20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V		−1	−1.6		−0.8	−1.2			−0.4				mA
					V_{IL} = 0.5 V												−2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX			−18		−55	−18		−55	−20		−100	−40		−100	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§I_I = −12 mA for SN54'/SN74' and −18 mA for 'LS13, 'LS14, 'LS132, and 'S132.

♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and 'S132, duration of output short-circuit should not exceed one second.

supply current¶

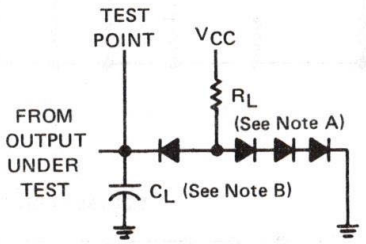
TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'13	14	23	20	32	8.5
'14	22	36	39	60	5.1
'132	15	24	26	40	5.1
'LS13	2.9	6	4.1	7	1.75
'LS14	8.6	16	12	21	1.72
'LS132	5.9	11	8.2	14	1.76
'S132	28	44	44	68	9

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A: typical values are at V_{CC} = 5 V, T_A = 25°C.

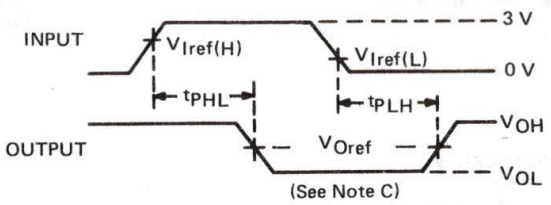
switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'13	C_L = 15 pF, R_L = 400 Ω		18	27		15	22
'14, '132			15	22		15	22
'LS13	C_L = 15 pF, R_L = 2 kΩ		15	22		18	27
'LS14			15	22		15	22
'LS132			15	22		15	22
'S132	C_L = 15 pF, R_L = 280 Ω		7	10.5		8.5	13

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. All diodes are 1N916 or 1N3064.
B. C_L includes probe and jrg capacitance.
C. Generator characteristics and reference voltages are:

	Generator Characteristics				Reference Voltages		
	Z_{out}	PRR	t_r	t_f	$V_{I\ ref(H)}$	$V_{I\ ref(L)}$	$V_{O\ ref}$
SN54'/SN74'	50 Ω	1 MHz	10 ns	10 ns	1.7 V	0.9 V	1.5 V
SN54LS'/SN74LS'	50 Ω	1 MHz	15 ns	6 ns	1.6 V	0.8 V	1.3 V
'S132	50 Ω	1 MHz	2.5 ns	2.5 ns	1.8 V	1.2 V	1.5 V

1076
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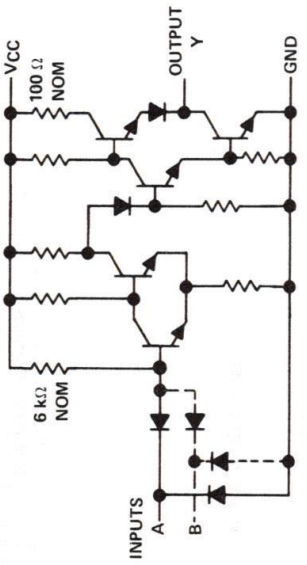
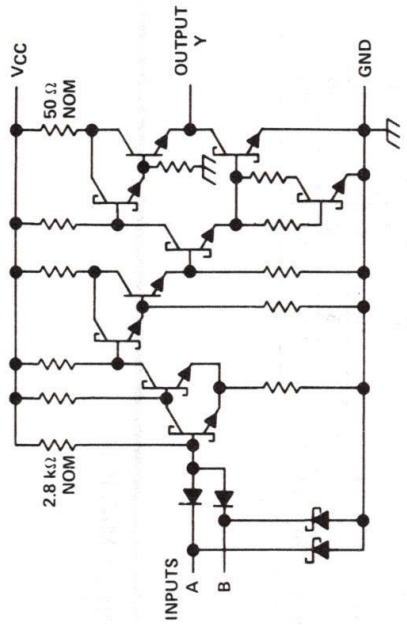
6-15

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

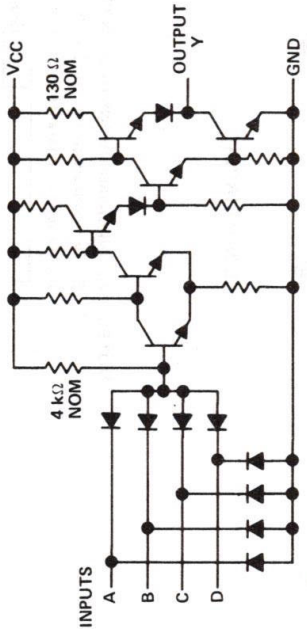
schematics (each gate)



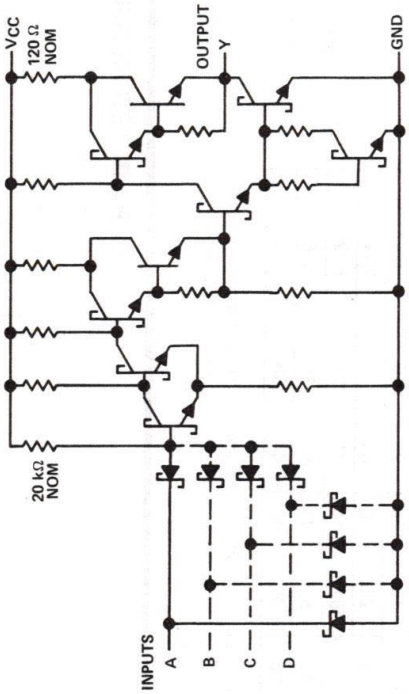
'14, '132 CIRCUITS



'S132 CIRCUITS



'13 CIRCUITS



'LS13, 'LS14, 'LS132 CIRCUITS

Resistor values shown are nominal.

TYPICAL CHARACTERISTICS OF '13, '14, AND '132 CIRCUITS†

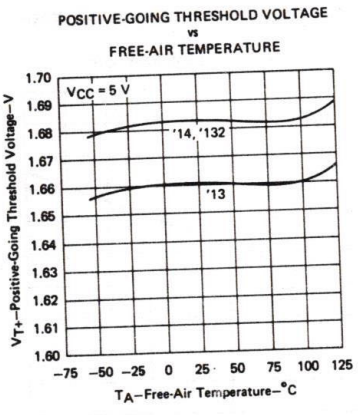


FIGURE 1

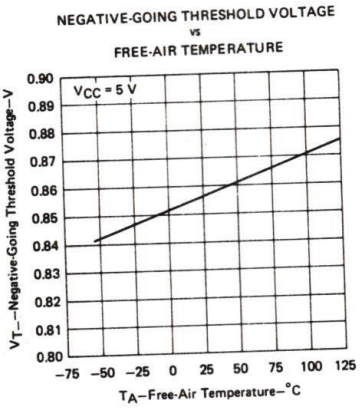


FIGURE 2

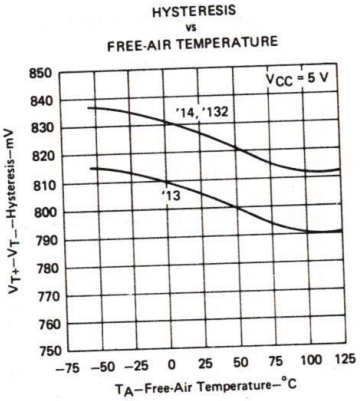


FIGURE 3

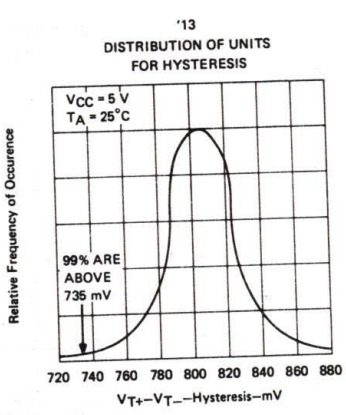


FIGURE 4

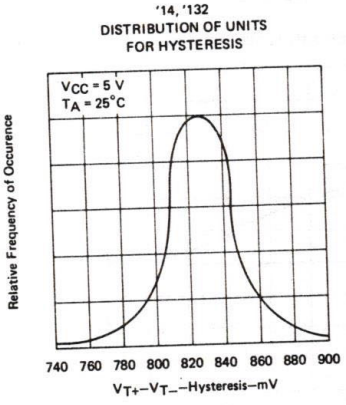


FIGURE 5

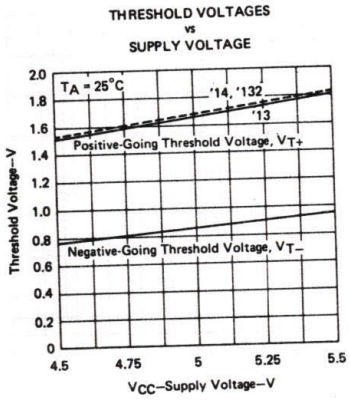


FIGURE 6

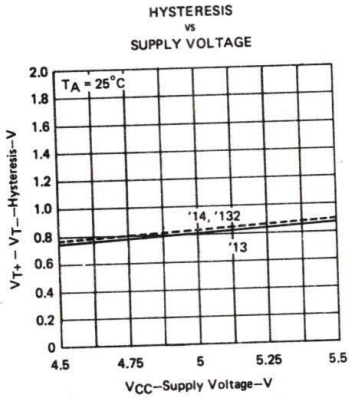


FIGURE 7

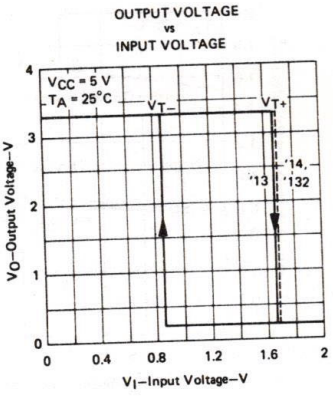
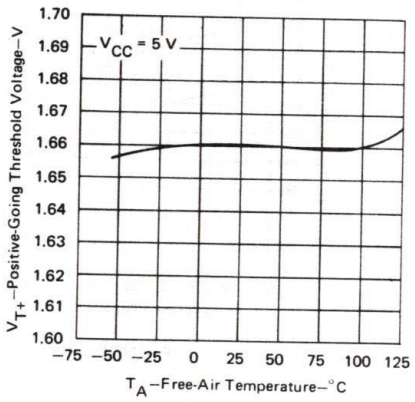


FIGURE 8

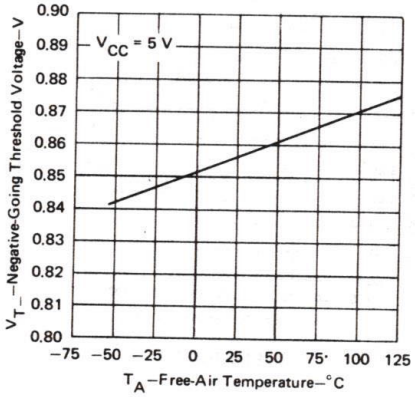
†Data for temperatures below 0°C and 70°C and supply voltages below 4.75V and above 5.25 V are applicable for SN5413, SN5414, and SN54132 only.

TYPICAL CHARACTERISTICS OF 'LS13, 'LS14, AND 'LS132 CIRCUITS†

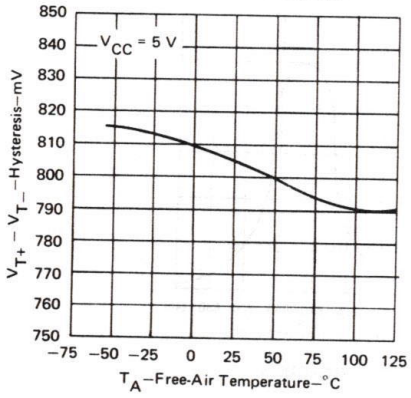
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



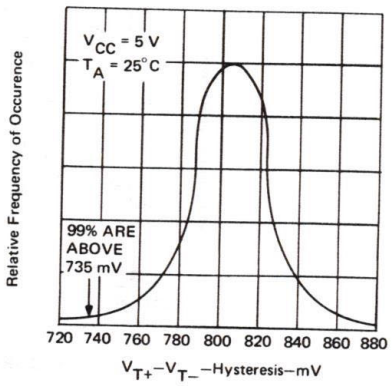
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



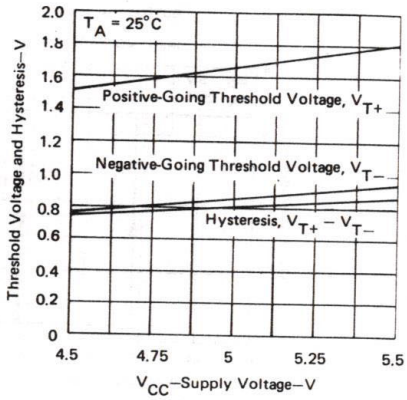
HYSTERESIS
vs
FREE-AIR TEMPERATURE



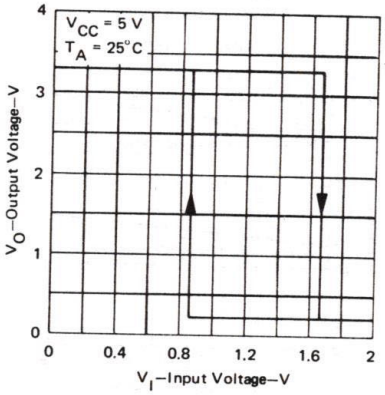
DISTRIBUTION OF UNITS
FOR HYSTERESIS



THRESHOLD VOLTAGES AND HYSTERESIS
vs
SUPPLY VOLTAGE

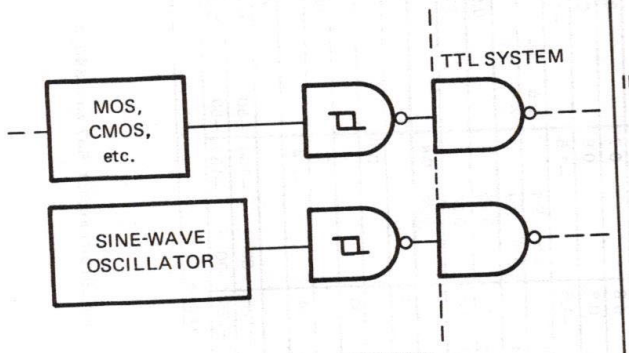


OUTPUT VOLTAGE
vs
INPUT VOLTAGE

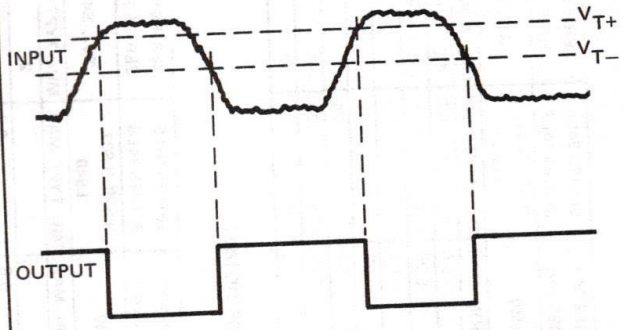


†Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 are applicable for SN54LS13, SN54LS14, and SN54LS132 only.

TYPICAL APPLICATION DATA

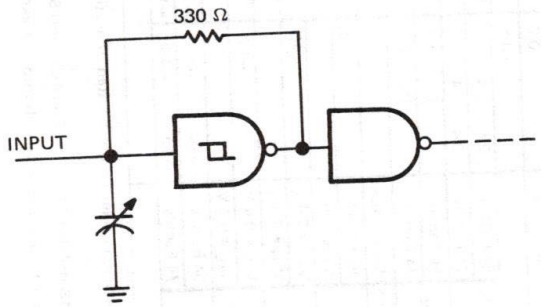


TTL SYSTEM INTERFACE
FOR SLOW INPUT WAVEFORMS

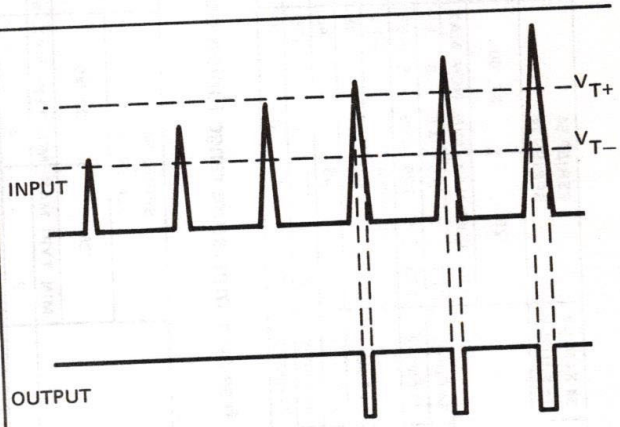


PULSE SHAPER

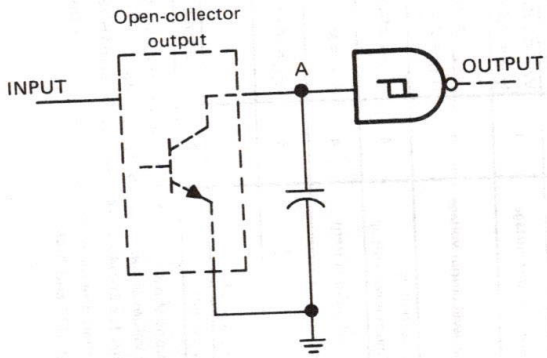
0.1 Hz to 10 MHz

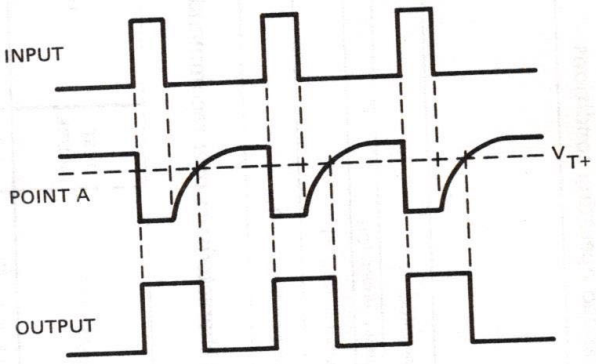


MULTIVIBRATOR



THRESHOLD DETECTOR





PULSE STRETCHER

6

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74						SERIES 54H SERIES 74H			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
		'28			'37, '40			'H40			'LS28, 'LS37 'LS40			'S37, 'S40			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				−2.4			−1.2			−1.5			−1.2			−3	mA
Low-level output current, I_{OL}	54 Family			48			48			60			12			60	mA
	74 Family			48			48			60			24			60	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74						SERIES 54H SERIES 74H			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
					'28			'37, '40			'H40			'LS28, 'LS37, 'LS40			'S37, 'S40			
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage	1, 2				2			2			2			2			2			V
V_{IL} Low-level input voltage	1, 2			54 Family			0.8			0.8			0.8			0.7			0.8	V
				74 Family			0.8			0.8			0.8			0.8			0.8	
V_{IK} Input clamp voltage	3	V_{CC} = MIN, I_I = §					−1.5			−1.5			−1.5			−1.5			−1.2	V
V_{OH} High-level output voltage	1	V_{CC} = MIN, I_{OH} = MAX	V_{IL} = V_{IL} max,	54 Family	2.4	3.4		2.4	3.3		2.4	3.4		2.5	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.4	3.3		2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL} Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
				74 Family		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 12 mA	Series 74LS											0.25	0.4				
I_I Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			1			0.1						1	mA
				V_I = 7 V												0.1				
I_{IH} High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			40			100							μA
				V_{IH} = 2.7 V												20			100	
I_{IL} Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			−1.6			−1.6			−4			−0.4				mA
				V_{IL} = 0.5 V															−4	
I_{OS} Short-circuit output current♦	6			54 Family	−70		−180	−20		−70	−40		−125	−30		−130	−50		−225	mA
I_{CC} Supply current	7	V_{CC} = MAX		74 Family	−70		−180	−18		−70	−40		−125	−30		−130	−50		−225	mA

See table on next page

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.

♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second for all of these circuits except 'S37 and 'S40, or 100 milliseconds for 'S37 and 'S40.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'28	12	21	33	57	5.63
'37	9	15.5	34	54	5.38
'40	4	8	17	27	5.25
'H40	10.4	16	25	40	8.85
'LS28	1.8	3.6	6.9	13.8	1.09
'LS37	0.9	2	6	12	0.86
'LS40	0.45	1	3	6	0.86
'S37	20	36	46	80	8.25
'S40	10	18	25	44	8.75

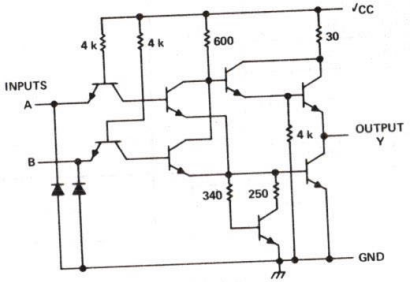
¶ Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

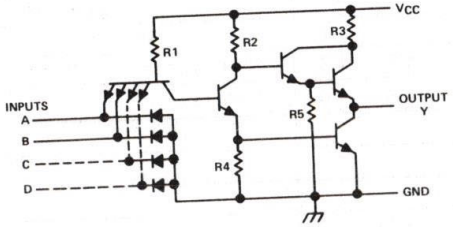
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low output		
		MIN	TYP	MAX	MIN	TYP	MAX
'28	C_L = 50 pF, R_L = 133 Ω		6	9		8	12
	C_L = 150 pF, R_L = 133 Ω		10	15		12	18
'37	C_L = 45 pF, R_L = 133 Ω		13	22		8	15
'40	C_L = 15 pF, R_L = 133 Ω		13	22		8	15
'H40	C_L = 25 pF, R_L = 93 Ω		8.5	12		6.5	12
'LS28	C_L = 45 pF, R_L = 667 Ω		12	24		12	24
'LS37			12	24		12	24
'LS40			12	24		12	24
'S37, 'S40	C_L = 50 pF, R_L = 93 Ω		4	6.5		4	6.5
	C_L = 150 pF, R_L = 93 Ω		6			6	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

schematics (each gate)

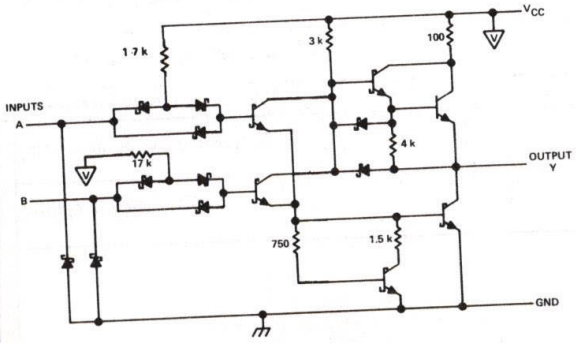


'28 CIRCUITS

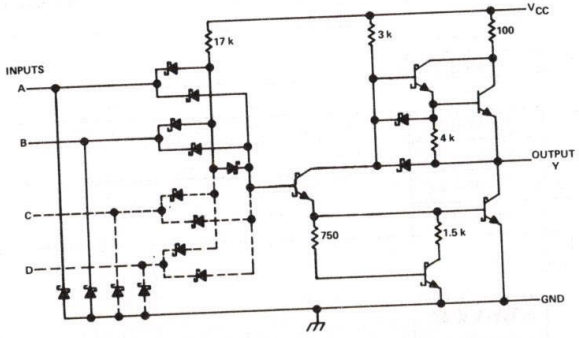


'37, '40, 'H40 CIRCUITS

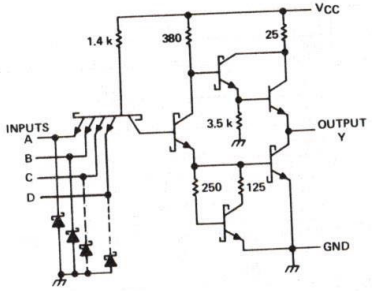
	'37	'40	'H40
R1	4 k	4 k	1.4 k
R2	600	600	390
R3	100	100	45
R4	400	400	250
R5	4 k	4 k	2 k



'LS28 CIRCUITS



'LS37, 'LS40 CIRCUITS



'S37, 'S40 CIRCUITS

Resistor values shown are nominal and in ohms.

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recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '128			SERIES 54S SERIES 74S 'S140			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−29			−40	mA
	74 Family			−42.4			−40	
Low-level output current, I_{OL}				48			60	mA
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	°C
	74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '128			SERIES 54S SERIES 74S 'S140			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			V
V_{IL}	Low-level input voltage	1, 2					0.8			0.8	V
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §				−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −2.4 mA	54 Family	2.4	3.4					V
				74 Family	2.4	3.4					
			V_{CC} = MIN, V_{IL} = 0.4 V, I_{OH} = −13.2 mA		2.4						
			V_{CC} = MIN, V_{IL} = 0.4 V, I_{OH} = MAX		2						
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −3 mA	54 Family				2.5	3.4		
				74 Family				2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.5 V, R_O = 50 Ω to GND					2			
I_I	Input current at maximum input voltage	4	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX			0.26	0.4			0.5	V
I_{IH}	High-level input current	4	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
			V_{CC} = MAX	V_{IH} = 2.4 V			40				μA
				V_{IH} = 2.7 V						100	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.4 V			−1.6				mA
				V_{IL} = 0.5 V						−4	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		−70		−180	−50		−225	mA
I_{CC}	Supply current, Total, outputs high	7	V_{CC} = MAX			12	21		10	18	mA
	Total, outputs low					33	57		25	44	
	Average per gate		V_{CC} = 5 V, 50% duty cycle			5.63			8.75		

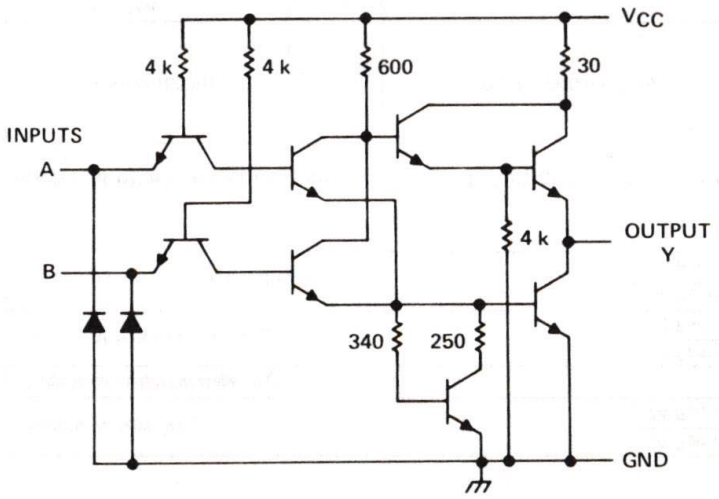
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for '128 and −18 mA for 'S140.
♦Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second for '128 or 100 milliseconds for 'S140.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

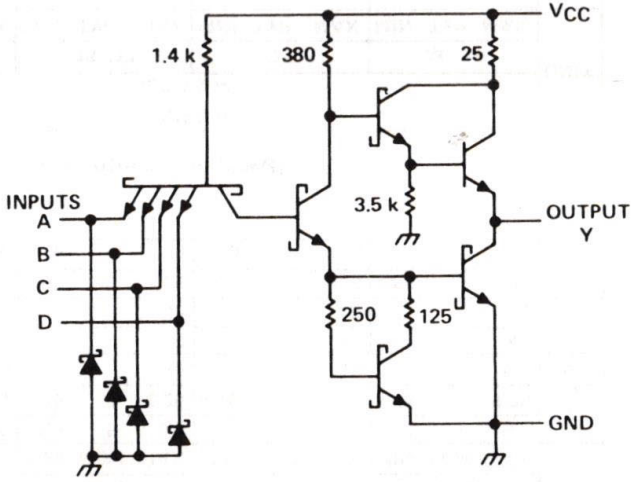
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'128	C_L = 50 pF, R_L = 133 Ω		6	9		8	12
	C_L = 150 pF, R_L = 133 Ω		10	15		12	18
'S140	C_L = 50 pF, R_L = 93 Ω		4	6.5		4	6.5
	C_L = 150 pF, R_L = 93 Ω		6			6	

#Load circuit and voltage waveforms are shown on page 3-10.

schematics (each driver)



'128 CIRCUITS



'S140 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54' / SERIES 74'												UNIT
		'06, '07			'16, '17			'26			'33, '38			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				30			15			15			5.5	V
Low-level output current, I_{OL}	54 Family			30			30			16			48	mA
	74 Family			40			40			16			48	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54' / SERIES 74'												UNIT
					'06, '07			'16, '17			'26			'33, '38			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2					0.8			0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	3	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5			−1.5			−1.5	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_I = ▲	V_{OH} = 12 V									50				μA
				V_{OH} = MAX			250			250			1000			250	
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_I = ▲	I_{OL} = 16 mA			0.4			0.4			0.4				V
				I_{OL} = MAX			0.7			0.7			0.4			0.4	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX,	V_I = 5.5 V			1			1			1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX,	V_{IH} = 2.4 V			40			40			40			40	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX,	V_{IL} = 0.4 V			−1.6			−1.6			−1.6			−1.6	mA
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page												mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

▲The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'06, '16	30	48	32	51	5.17
'07, '17	29	41	21	30	4.17
'26	4	8	12	22	2.00
'33	12	21	33	57	5.63
'38	5	8.5	34	54	4.88

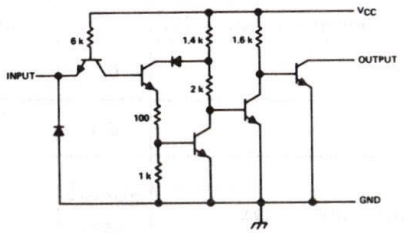
¶Maximum values of I_{CC} shown are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

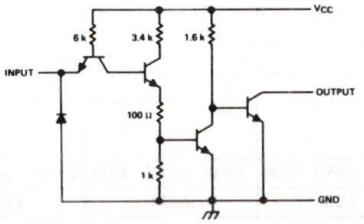
TYPE	TEST CONDITIONS#		t_{PLH} (ns) Propagation delay time, low-to-high-level output		t_{PHL} (ns) Propagation delay time, high-to-low-level output	
			TYP	MAX	TYP	MAX
'06, '16	C_L = 15 pF,	R_L = 110 Ω	10	15	15	23
'07, '17			6	10	20	30
'26	C_L = 15 pF,	R_L = 1 kΩ	16	24	11	17
'33	C_L = 50 pF,	R_L = 133 Ω	10	15	12	18
	C_L = 150 pF,	R_L = 133 Ω	15	22	16	24
'38	C_L = 45 pF,	R_L = 133 Ω	14	22	11	18

#Load circuit and voltage waveforms are shown on page 3-10.

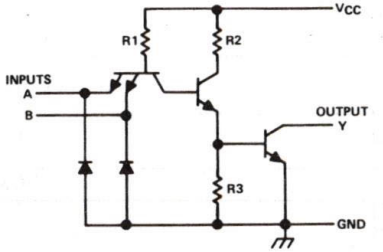
schematics (each gate)



'06, '16 CIRCUITS

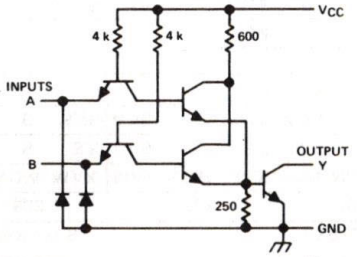


'07, '17 CIRCUITS



CIRCUITS	R1	R2	R3
'26	4 kΩ	1.6 kΩ	1 kΩ
'38	4 kΩ	600 Ω	400 Ω

'26, '38 CIRCUITS



'33 CIRCUITS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54LS' SERIES 74LS'									SERIES 54S' SERIES 74S'			UNIT
		'LS26			'LS33			'LS38			'S38			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				15			5.5			5.5			5.5	V
Low-level output current, I_{OL}	54 Family			4			12			12			60	mA
	74 Family			8			24			24			60	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54LS' SERIES 74LS'									SERIES 54S' SERIES 74S'			UNIT
						'LS26			'LS33			'LS38			'S38			
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.7			0.7			0.7			0.8	V
					74 Family			0.8			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I −18 mA					−1.5			−1.5			−1.5			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_I = ▲		V_{OH} = 12 V			50										μA
					V_{OH} = MAX			1000			250			250			250	
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_I = ▲	I_{OL} = MAX	54 Family	0.25		0.4	0.25		0.4	0.25		0.4			0.5	V
					74 Family	0.35		0.5	0.35		0.5	0.35		0.5			0.5	
				I_{OL} = 4 mA	Series 74LS'	0.25		0.4										
				I_{OL} = 12 mA					0.25		0.4	0.25		0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V												1	mA
					V_I = 7 V			0.1			0.1			0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.7 V			20			20			20			100	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			−0.4			−0.4			−0.4				mA
					V_{IL} = 0.5 V												−4	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page												mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
▲The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.

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supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'LS26	0.8	1.6	2.4	4.4	0.4
'LS33	1.8	3.6	6.9	13.8	1.09
'LS38	0.9	2	6	12	0.86
'S38	20	36	46	80	8.25

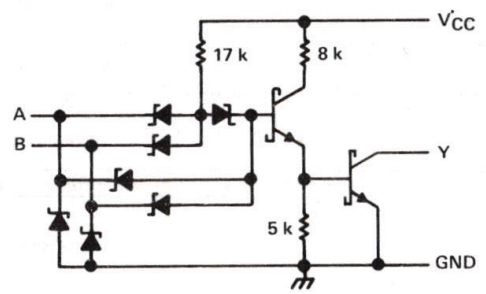
¶Maximum values of I_{CC} shown are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

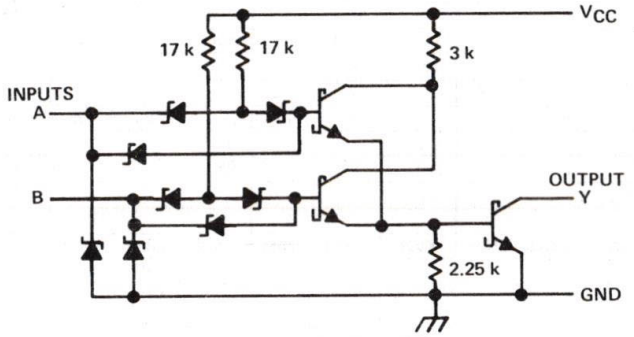
TYPE	TEST CONDITIONS#		t_{PLH} (ns) Propagation delay time, low-to-high-level output		t_{PHL} (ns) Propagation delay time, high-to-low-level output	
			TYP	MAX	TYP	MAX
'LS26	C_L = 15 pF,	R_L = 2 kΩ	17	32	15	28
'LS33	C_L = 45 pF,	R_L = 667 Ω	20	32	18	28
'LS38			20	32	18	28
'S38	R_L = 93 Ω	C_L = 50 pF	6.5	10	6.5	10
		C_L = 150 pF	9		8.5	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

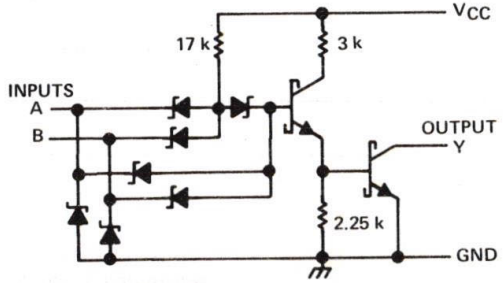
schematics (each gate)



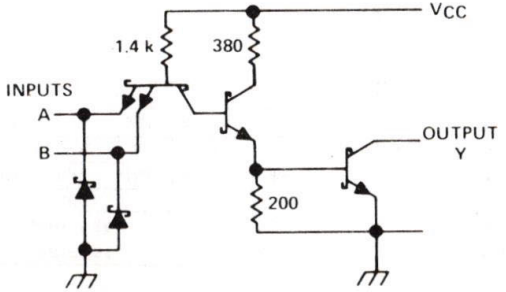
'LS26 CIRCUITS



'LS33 CIRCUITS



'LS38 CIRCUITS



'S38 CIRCUITS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '32			SERIES 54LS SERIES 74LS 'LS32			SERIES 54S SERIES 74S 'S32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				−800			−400			−1000	μA
Low-level output current, I_{OL}	54 Family			16			4			20	mA
	74 Family			16			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '32			SERIES 54LS SERIES 74LS 'LS32			SERIES 54S SERIES 74S 'S32			UNIT
							MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		1, 2				2			2			2			V
V_{IL}	Low-level input voltage		1, 2			54 Family			0.8			0.7			0.8	V
						74 Family			0.8			0.8			0.8	
V_{IK}	Input clamp voltage		3	V_{CC} = MIN,	I_I = §				−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage		1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = MAX		54 Family	2.4	3.4		2.5	3.4		2.5	3.4		V
						74 Family	2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		2	V_{CC} = MIN, V_{IL} = V_{IL} max	I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4			0.5	V
						74 Family		0.2	0.4		0.35	0.5			0.5	
					I_{OL} = 4 mA	Series 74LS					0.25	0.4				
I_I	Input current at maximum input voltage		4	V_{CC} = MAX		V_I = 5.5 V			1						1	mA
						V_I = 7 V						0.1				
I_{IH}	High-level input current		4	V_{CC} = MAX		V_{IH} = 2.4 V			40							μA
						V_{IH} = 2.7 V						20			50	
I_{IL}	Low-level input current		5	V_{CC} = MAX		V_{IL} = 0.4 V			−1.6			−0.4				mA
						V_{IL} = 0.5 V									−2	
I_{OS}	Short-circuit output current♦		6	V_{CC} = MAX		54 Family	−20		−55	−20		−100	−40		−100	mA
						74 Family	−18		−55	−20		−100	−40		−100	
I_{CC}	Supply current	Total, outputs high	7	V_{CC} = MAX				15	22		3.1	6.2		18	32	mA
		Total, outputs low						23	38		4.9	9.8		38	68	
		Average per gate		V_{CC} = 5 V,	50% duty cycle			4.75			1.0			7		

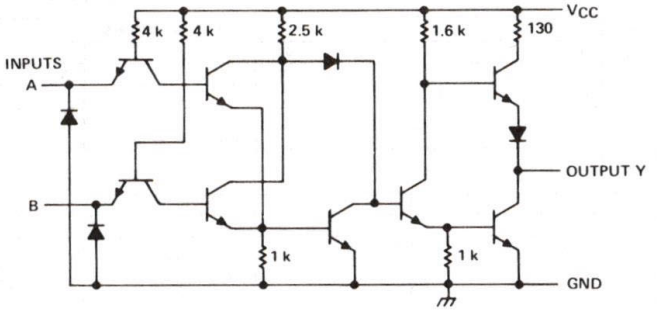
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of the short-circuit should be less than one second.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

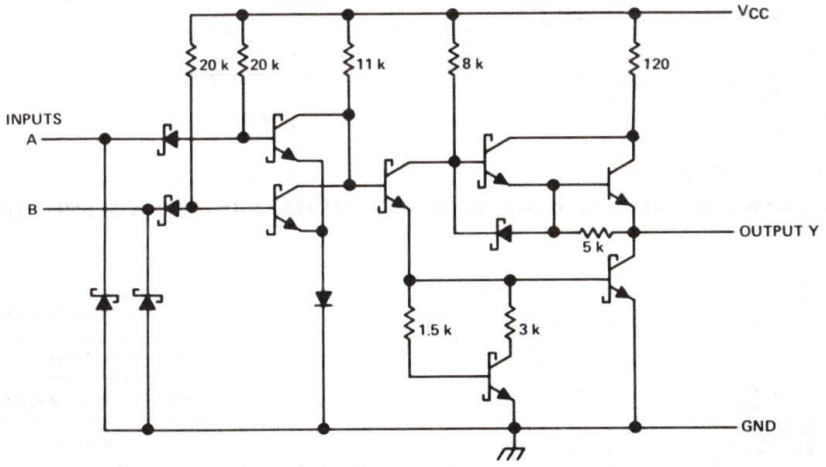
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'32	C_L = 15 pF, R_L = 400 Ω		10	15		14	22
'LS32	C_L = 15 pF, R_L = 2 kΩ		14	22		14	22
'S32	C_L = 15 pF, R_L = 280 Ω		4	7		4	7
	C_L = 50 pF, R_L = 280 Ω		5			5	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

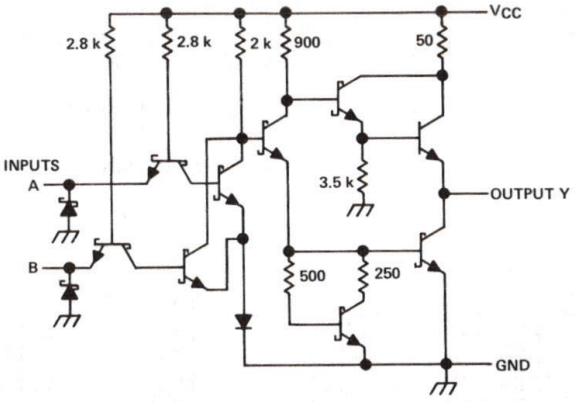
schematics (each gate)



'32 CIRCUITS



'LS32 CIRCUITS



'S32 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '51, '54			SERIES 54H SERIES 74H 'H51, 'H54			SERIES 54L SERIES 74L 'L51, 'L54, 'L55			SERIES 54LS SERIES 74LS 'LS51, 'LS54, 'LS55			SERIES 54S SERIES 74S 'S51, 'S64			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}		54 Family			−400			−500			−100			−400			−1000	μA
		74 Family			−400			−500			−200			−400			−1000	
Low-level output current, I_{OL}		54 Family			16			20			2			4			20	mA
		74 Family			16			20			3.6			8			20	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '51, '54			SERIES 54H SERIES 74H 'H51, 'H54			SERIES 54L SERIES 74L 'L51, 'L54, 'L55			SERIES 54LS SERIES 74LS 'LS51, 'LS54, 'LS55			SERIES 54S SERIES 74S 'S51, 'S64			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.8			0.7			0.7			0.8	V
					74 Family			0.8			0.8			0.7			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN,	I_I = §				−1.5			−1.5						−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX		54 Family	2.4	3.4		2.4	3.4		2.4	3.3		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS											0.25	0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			1			0.1						1	mA
					V_I = 7 V												0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			50			10							μA
					V_{IH} = 2.7 V												20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.3 V									−0.18							mA
					V_{IL} = 0.4 V			−1.6			−2						−0.4				
					V_{IL} = 0.5 V															−2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		54 Family	−20		−55	−40		−100	−3		−15	−20		−100	−40		−100	mA
					74 Family	−18		−55	−40		−100	−3		−15	−20		−100	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page															mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.

♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS', SN54H'/SN74H', and SN54S'/SN74S', duration of the short-circuit should not exceed one second.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per AOI gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'51	4	8	7.4	14	2.85
'54	4	8	5.1	9.5	4.55
'H51	8.2	12.8	15.2	24	5.85
'H54	7.1	11	9.4	14	8.25
'L51	0.44	0.8	0.76	1.3	0.30
'L54	0.39	0.8	0.60	0.99	0.50
'L55	0.22	0.4	0.38	0.65	0.30
'LS51	0.8	1.6	1.4	2.8	0.55
'LS54	0.8	1.6	1.0	2	0.9
'LS55	0.4	0.8	0.7	1.3	0.55
'S51	8.2	17.8	13.6	22	5.45
'S64	7	12.5	8.5	16	7.75

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

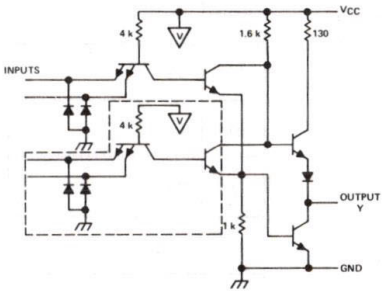
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'51, '54	C_L = 15 pF, R_L = 400 Ω		13	22		8	15
'H51	C_L = 25 pF, R_L = 280 Ω		6.8	11		6.2	11
'H54	C_L = 25 pF, R_L = 280 Ω		7	11		6.2	11
'L51, 'L54, 'L55	C_L = 50 pF, R_L = 4 kΩ		50	90		35	60
'LS51, 'LS55	C_L = 15 pF, R_L = 2 kΩ		12	20		12.5	20
'LS54	C_L = 15 pF, R_L = 2 kΩ		12	20		12.5	20
'S51, 'S64	C_L = 15 pF, R_L = 280 Ω		3.5	5.5		3.5	5.5
	C_L = 50 pF, R_L = 280 Ω		5			5.5	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

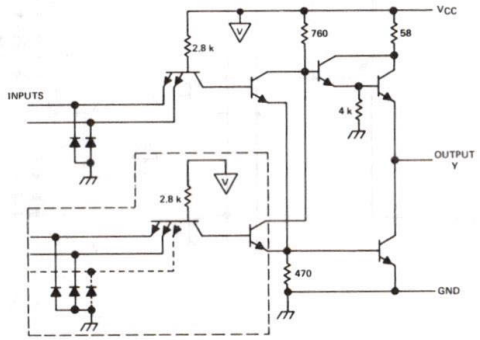
schematics (each gate)

The portion of the circuits within the dashed lines is repeated (with as many emitters or input diodes as applicable) for each additional AND section.

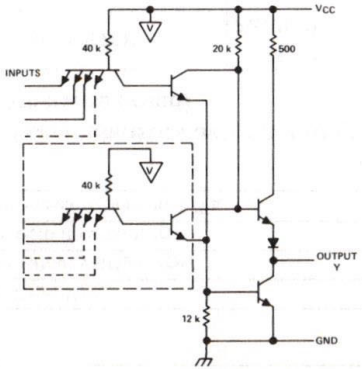
Resistor values shown are nominal and in ohms.



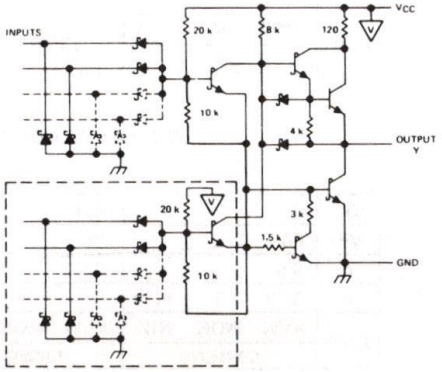
'51, '54 CIRCUITS



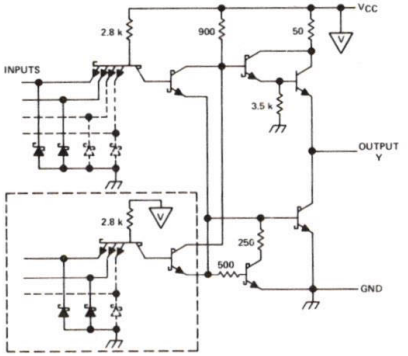
'H51, 'H54 CIRCUITS



'L51, 'L54, 'L55 CIRCUITS



'LS51, 'LS54, 'LS55 CIRCUITS



'S51, 'S64 CIRCUITS

recommended operating conditions

	SN54S65			SN74S65			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	'S65			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2		2			V
V_{IL}	Low-level input voltage	1, 2				0.8	V
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IH} = 0.8 V, V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 2 V, I_{OL} = 20 mA			0.5	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX, V_I = 2.7 V			50	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX, V_I = 0.5 V			−2	mA
I_{CCH}	Supply current, output high	7	V_{CC} = MAX		6	11	mA
I_{CCL}	Supply current, output low	7	V_{CC} = MAX		8.5	16	mA

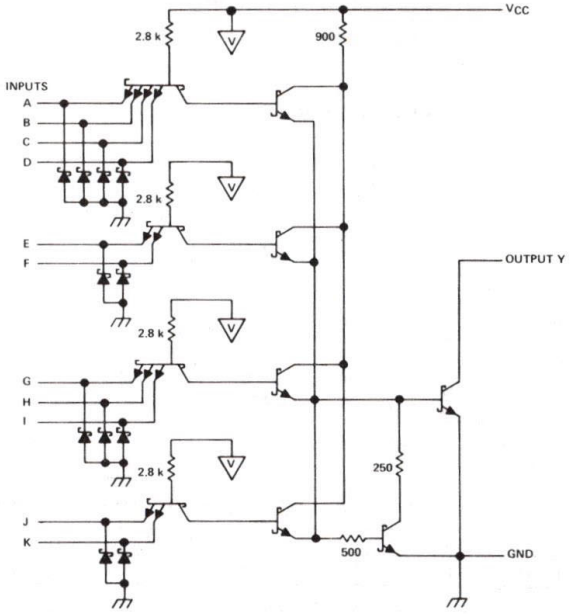
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS#	'S65			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	2	5	7.5	ns
		C_L = 50 pF, R_L = 280 Ω		8		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω	2	5.5	8.5	ns
		C_L = 50 pF, R_L = 280 Ω		6.5		ns

#Load circuit and voltage waveforms are shown on page 3-10.

schematic



Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '125, '126, '425, '426			SERIES 54LS / SERIES 74LS 'LS125A, 'LS126A			SERIES 54S / SERIES 74S 'S134			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−2			−1			−2	mA
	74 Family			−5.2			−2.6			−6.5	
Low-level output current, I_{OL}	54 Family			16			12			20	mA
	74 Family			16			24			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 / SERIES 74 '125, '126, '425, '426			SERIES 54LS / SERIES 74LS 'LS125A, 'LS126A			SERIES 54S / SERIES 74S 'S134			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN,		I_I = §			−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX	54 Family	2.4	3.3		2.4			2.4	3.4		V
					74 Family	2.4	3.1		2.4			2.4	3.2		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = MAX	54 Family			0.4		0.25	0.4			0.5	V
					74 Family			0.4		0.35	0.5			0.5	
				I_{OL} = 12 mA	Series 74LS					0.25	0.4				
I_{OZ}	Off-state (high-impedance state) output current	19	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max		V_O = 2.4 V			40			20			50	μA
					V_O = 0.4 V			−40			−20				
					V_O = 0.5 V									−50	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1						1	mA
					V_I = 7 V						0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40							μA
					V_{IH} = 2.7 V						20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			−1.6			0.4				mA
					V_{IL} = 0.5 V									−2	
I_{OS}	Short-circuit output current◆	6	V_{CC} = MAX		54 Family	−30		−70	−40		−225	−40		−100	mA
					74 Family	−28		−70	−40		−225	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page									mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.

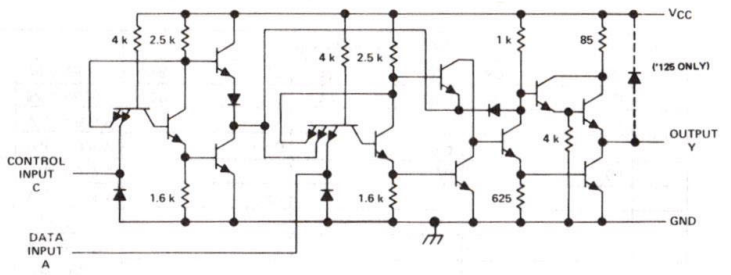
◆Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of the short circuit should not exceed one second.

supply current¶

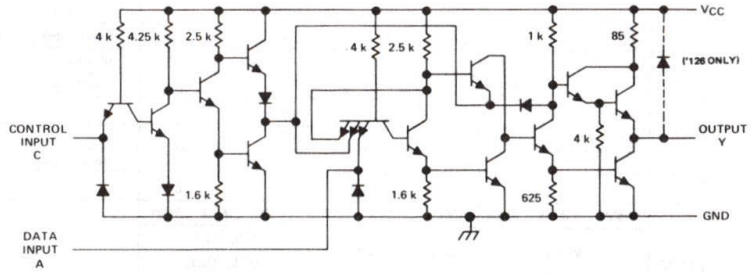
TYPE	TEST CONDITIONS		I_{CC} (mA)		
	DATA INPUTS	OUTPUT CONTROLS	MIN	TYP	MAX
'125, '425	0 V	4.5 V		32	54
'126, '426	0 V	0 V		36	62
'LS125A	0 V	4.5 V		11	20
'LS126A	0 V	0 V		12	22
'S134	0 V	0 V		7	13
	5 V	0 V		9	16
	5 V	5 V		14	25

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)



'125, '425 CIRCUITS



'126, 426 CIRCUITS

Resistor values shown are nominal and in ohms.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		SERIES 54/74				SERIES 54LS/74LS				SERIES 54S/74S			UNIT
		TEST CONDITIONS#	'125, '425 TYP	'125, '425 MAX	'126, '426 TYP	'126, '426 MAX	TEST CONDITIONS#	'LS125A TYP	'LS125A MAX	'LS126A TYP	'LS126A MAX	TEST CONDITIONS#	'S134 TYP	'S134 MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 400 Ω	8	13	8	13	C_L = 45 pF, R_L = 667 Ω	9	15	9	15	C_L = 15 pF, R_L = 280 Ω	4	6	ns
												C_L = 50 pF, R_L = 280 Ω	5.5		
t_{PHL}	Propagation delay time, high-to-low-level output		12	18	12	18		7	18	8	18	C_L = 15 pF, R_L = 280 Ω	5	7.5	ns
												C_L = 50 pF, R_L = 280 Ω	7		
t_{PZH}	Output enable time to high level		11	17	11	18		12	20	16	25	C_L = 50 pF, R_L = 280 Ω	13	19.5	ns
t_{PZL}	Output enable time to low level		16	25	16	25		15	25	21	35		14	21	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF, R_L = 400 Ω	5	8	10	16	C_L = 5 pF, R_L = 667 Ω		20		25	C_L = 5 pF, R_L = 280 Ω	5.5	8.5	ns
t_{PLZ}	Output disable time from low level		7	12	12	18			20		25		9	14	ns

#Load circuit and voltage waveforms are shown on page 3-10 and 3-11.

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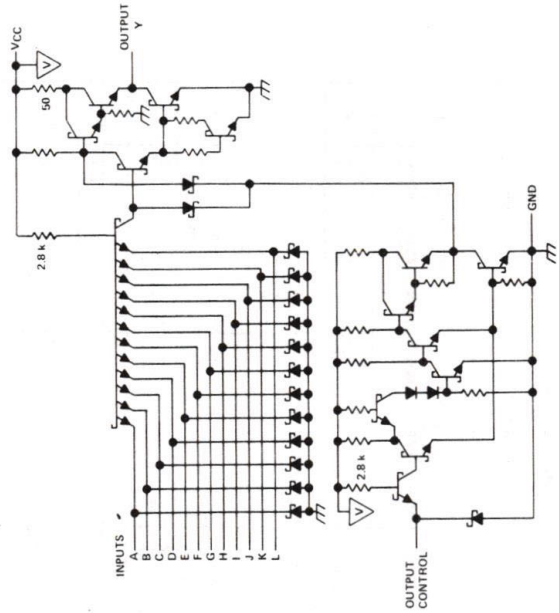
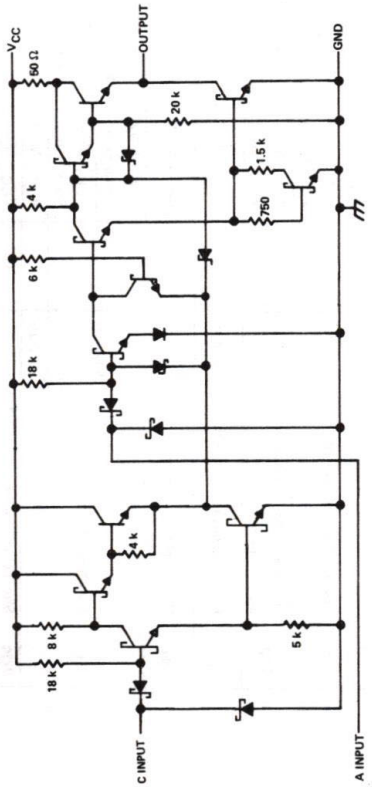
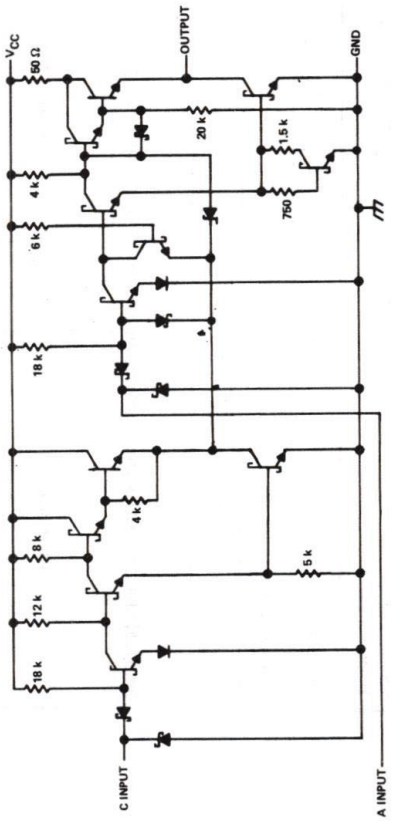
schematics (each gate)



'S134 CIRCUITS



'LS125A CIRCUITS



'LS126A CIRCUITS

Resistor values shown are nominal and in ohms.

6

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '365A, '366A '367A, '368A			SERIES 54LS SERIES 74LS 'LS365A, 'LS366A 'LS367A, 'LS368A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−2			−1	mA
	74 Family			−5.2			−2.6	
Low-level output current, I_{OL}	54 Family			32			12	mA
	74 Family			32			24	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	°C
	74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '365A, '366A '367A, '368A			SERIES 54LS SERIES 74LS 'LS365A, 'LS366A 'LS367A, 'LS368A			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.7	V
					74 Family			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN,	I_I = §				−1.5			−1.5	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX	54 Family	2.4	3.3		2.4	3.3		V
					74 Family	2.4	3.1		2.4	3.1		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = MAX	54 Family			0.4		0.25	0.4	V
					74 Family			0.4		0.35	0.5	
			V_{IL} = V_{IL} max	I_{OL} = 12 mA	Series 74LS					0.25	0.4	
I_{OZ}	Off-state (high-impedance state) output current	19	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V,	V_O = 2.4 V			40			20	μA
					V_O = 0.4 V			−40			−20	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1				mA
					V_I = 7 V						0.1	
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40				μA
					V_{IH} = 2.7 V						20	
I_{IL}	Low-level input current	A inputs	V_{CC} = MAX, V_I = 0.5 V, Either $\overline{G}$ input at 2 V					−40			−20	μA
			V_{CC} = MAX, V_I = 0.4 V, Both $\overline{G}$ inputs at 0.4 V					−1.6			−0.4	mA
		$\overline{G}$ inputs	V_{CC} = MAX, V_I = 0.4 V,					−1.6			−0.4	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX			−40		−130	−40		−225	mA
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page						mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS', SN54S/SN74S'.

♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of output short-circuit should not exceed one second.

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supply current¶

TYPE	DATA INPUTS	OUTPUT CONTROLS	I_{CC} (mA)	
			TYP	MAX
'365A, '367A	0 V	4.5 V	65	85
'366A, '368A	0 V	4.5 V	59	77
'LS365A, 'LS367A	0 V	4.5 V	14	24
'LS366A, 'LS368A	0 V	4.5 V	12	21

¶ Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

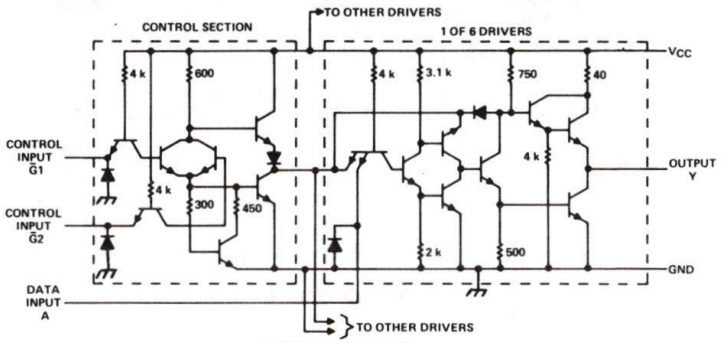
switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 1

PARAMETER*	TEST CONDITIONS	SERIES 54/74 '365A, '367A TYP	SERIES 54/74 '365A, '367A MAX	SERIES 54/74 '366A, '368A TYP	SERIES 54/74 '366A, '368A MAX	TEST CONDITIONS	SERIES 54LS/74LS 'LS365A, 'LS367A TYP	SERIES 54LS/74LS 'LS365A, 'LS367A MAX	SERIES 54LS/74LS 'LS366A, 'LS368A TYP	SERIES 54LS/74LS 'LS366A, 'LS368A MAX
t_{PLH}	C_L = 50 pF, R_L = 400 Ω		16		17	C_L = 45 pF, R_L = 667 Ω	10	16	7	15
t_{PHL}			22		16		9	22	12	18
t_{PZH}			35		35		19	35	18	35
t_{PZL}			37		37		24	40	28	45
t_{PHZ}	C_L = 5 pF, R_L = 400 Ω		11		11	C_L = 5 pF, R_L = 667 Ω		30		32
t_{PLZ}			27		27			35		35

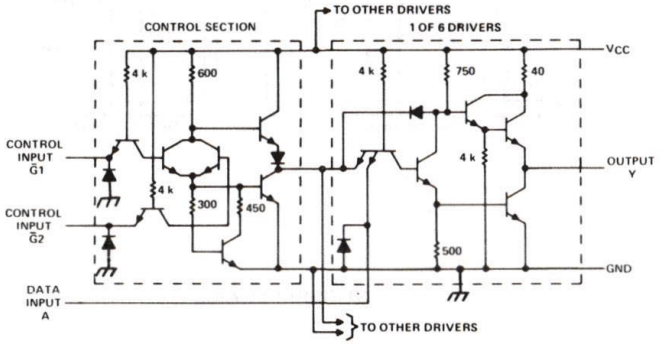
*t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PZH} = Output enable time to high level
t_{PZL} = Output enable time to low level
t_{PHZ} = Output disable time from high level
t_{PLZ} = Output disable time from low level

NOTE 1: Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

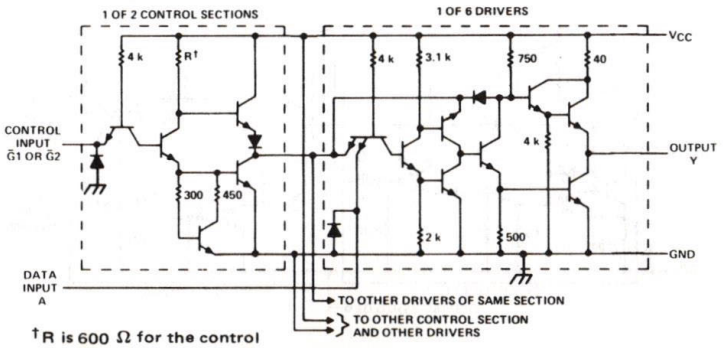
schematics



'365A CIRCUITS

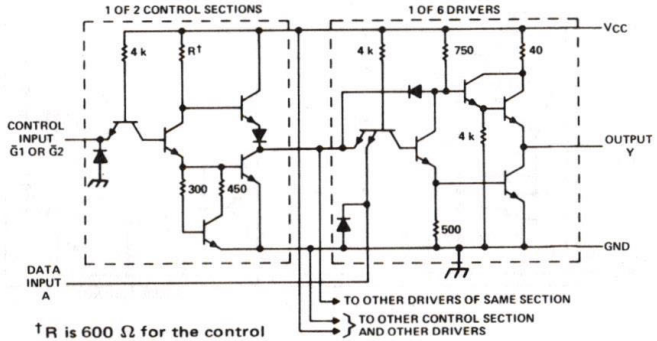


'366A CIRCUITS



†R is 600 Ω for the control section associated with $\overline{G}1$ and 900 Ω for the control section associated with $\overline{G}2$.

'367A CIRCUITS



†R is 600 Ω for the control section associated with $\overline{G}1$ and 900 Ω for the control section associated with $\overline{G}2$.

'368A CIRCUITS

Resistor values shown are nominal and in ohms.

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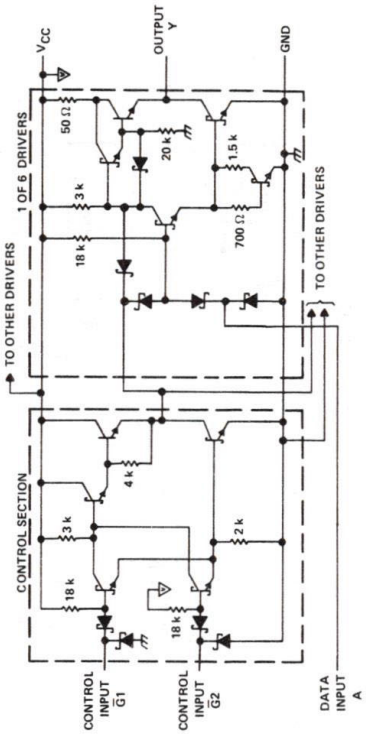
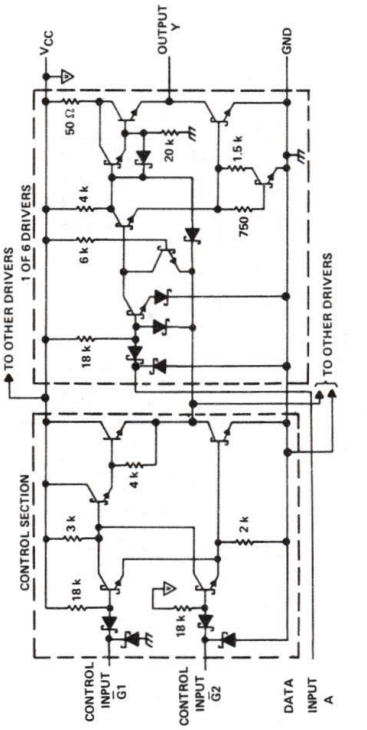
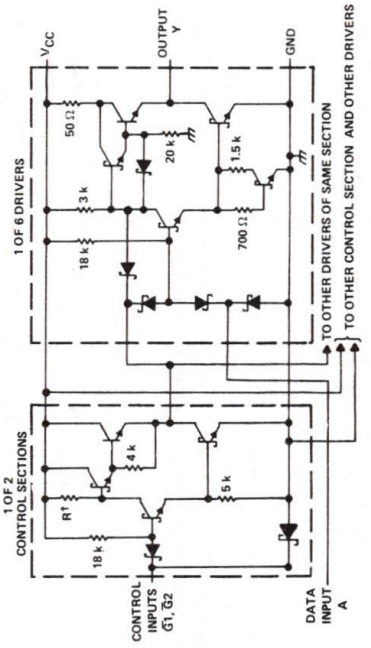


'LS366A CIRCUITS

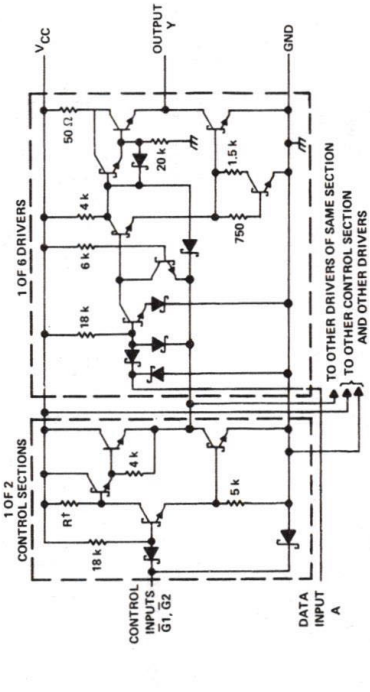


'LS365A CIRCUITS



'LS368A CIRCUITS

† R is 5 kΩ for the control section associated with $\overline{G}1$ and 8 kΩ for the control section associated with $\overline{G}2$.



'LS367A CIRCUITS

† R is 5 kΩ for the control section associated with $\overline{G}1$ and 8 kΩ for the control section associated with $\overline{G}2$.

Resistor values shown are nominal and in ohms

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recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74						SERIES 54H SERIES 74H			UNIT
			'23			'50, '53			'H50, 'H52, 'H53, 'H55			
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−800			−400			−500	μA
Low-level output current, I_{OL}		54 Family			16			16			20	mA
		74 Family			16			16			20	
Operating free-air temperature range, T_A		54 Family	−55		125	−55		125	−55		125	°C
		74 Family	0		70	0		70	0		70	

The '23, '50, and '53 are designed for use with up to four '60 expanders.
The 'H50, 'H53, and 'H55 are designed for use with up to four 'H60 expanders or one 'H62 expander.
The 'H52 is designed for use with up to six 'H61 expanders.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74						SERIES 54H SERIES 74H			UNIT
					'23			'50, '53			'H50, 'H52 'H53, 'H55			
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §				−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_I = ▲,	I_{OH} = MAX	2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_I = ▲,	I_{OL} = MAX		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current, Data input	4	V_{CC} = MAX, V_{IH} = 2.4 V				40			40			50	μA
	High-level input current, Strobe of '23						160							
I_{IL}	Low-level input current, Data inputs	5	V_{CC} = MAX, V_{IL} = 0.4 V				−1.6			−1.6			−2	mA
	Low-level input current, Strobe of '23						−6.4							
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX	54 Family	−20		−55	−20		−55	−40		−100	mA
				74 Family	−18		−55	−18		−55	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page									mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74' and −8 mA for SN54H'/SN74H'.
▲The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.
♦Not more than one output should be shorted at a time, and for the SN54H'/SN74H', duration of short-circuit should not exceed one second.

electrical characteristics using expander inputs, V_{CC} = MIN, T_A = MIN (unless otherwise noted)

TYPE	$I_{\overline{X}}$ (mA) (I_X for 'H52) Expander current			$V_{BE(Q)}$ (V) Base-emitter voltage of output transistor Q			V_{OH} (V) High-level output voltage			V_{OL} (V) Low-level output voltage		
	TEST CONDITIONS	MIN	TYP‡ MAX	TEST CONDITIONS	MIN	TYP‡ MAX	TEST CONDITIONS	MIN	TYP‡ MAX	TEST CONDITIONS	MIN	TYP‡ MAX
SN5423	$V_{\overline{X}X}$ = 0.4 V, I_{OL} = 16 mA, See Figure 10		−3.5	$I_X + I_{\overline{X}}$ = 410 μA, $R_{\overline{X}X}$ = 0, I_{OL} = 16 mA, See Figure 11		1.1	I_X = 150 μA, $I_{\overline{X}}$ = −150 μA, I_{OH} = −400 μA, See Figure 12	2.4	3.4	$I_X + I_{\overline{X}}$ = 300 μA, $R_{\overline{X}X}$ = 114 Ω▲ I_{OL} = 16 mA, See Figure 11		0.2 0.4
SN5450			−2.9									
SN5453			−2.9									
SN7423	$V_{\overline{X}X}$ = 0.4 V, I_{OL} = 16 mA, See Figure 10		−3.8	$I_X + I_{\overline{X}}$ = 620 μA, $R_{\overline{X}X}$ = 0, I_{OL} = 16 mA, See Figure 11		1	I_X = 270 μA, $I_{\overline{X}}$ = −270 μA, I_{OH} = −400 μA, See Figure 12	2.4	3.4	$I_X + I_{\overline{X}}$ = 430 μA, $R_{\overline{X}X}$ = 105 Ω▲ I_{OL} = 16 mA, See Figure 11		0.2 0.4
SN7450			−3.1									
SN7453			−3.1									
SN54H50, SN54H53, SN54H55	$V_{\overline{X}}$ = 1.4 V, I_X = 0, I_{OL} = 0, See Figure 10		−5.85	$I_X + I_{\overline{X}}$ = 700 μA, $R_{\overline{X}X}$ = 0, I_{OL} = 20 mA, See Figure 11		1.1	I_X = 320 μA, $I_{\overline{X}}$ = −320 μA, I_{OH} = −500 μA, See Figure 12	2.4	3.4	$I_X + I_{\overline{X}}$ = 470 μA, $R_{\overline{X}X}$ = 68 Ω, I_{OL} = 20 mA, See Figure 11		0.2 0.4
SN74H50, SN74H53, SN74H55	$V_{\overline{X}}$ = 1.4 V, I_X = 0, I_{OL} = 0, See Figure 10		−6.3	$I_X + I_{\overline{X}}$ = 1.1 mA, $R_{\overline{X}X}$ = 0, I_{OL} = 20 mA, See Figure 11		1	I_X = 570 μA, I_X = −570 μA, I_{OH} = −500 μA, See Figure 12	2.4	3.4	$I_X + I_{\overline{X}}$ = 600 μA, $R_{\overline{X}X}$ = 63 Ω, I_{OL} = 20 mA, See Figure 11		0.2 0.4
SN54H52	V_X = 1 V, I_{OH} = −500 μA, See Figure 13	−2.7	−4.5				V_X = 1 V, I_{OH} = −500 μA, See Figure 13	2.4	3.4	I_X = −300 μA, I_{OL} = 20 mA, T_A = MAX, See Figure 14		0.2 0.4
SN74H52		−2.9	−5.35									

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

▲$R_{\overline{X}X}$ equals 114 Ω for SN5423, 138 Ω for SN5450 and SN5453, 105 Ω for SN7423, and 130 Ω for SN7450 and SN7453.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'23	8	16	10	19	4.5
'50	4	8	7.4	14	2.85
'53	4	8	5.1	9.5	4.55
'H50	8.2	12.8	15.2	24	5.85
'H52	20	31	15.2	24	17.6
'H53	7.1	11	9.4	14	8.25
'H55	4.5	6.4	7.5	12	6.00

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

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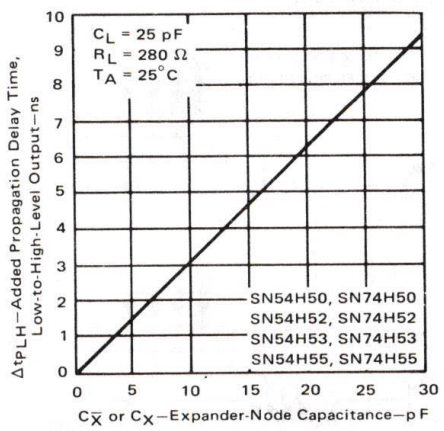
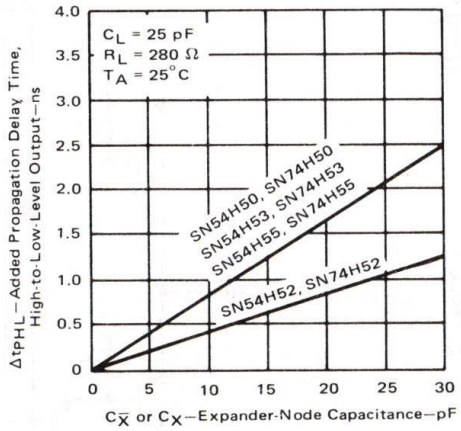
switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output		t_{PHL} (ns) Propagation delay time, high-to-low-level output	
		TYP	MAX	TYP	MAX
'23, '50, '53	C_L = 15 pF, R_L = 400 Ω, Expander pins open	13	22	8	15
'50	C_L = 15 pF, R_L = 400 Ω, From input of '60 expander	15	30	10	20
'H50	C_L = 25 pF, R_L = 280 Ω, Expander pins open	6.8	11	6.2	11
'H52		10.6	15	9.2	15
'H53		7	11	6.2	11
'H55		7	11	6.5	11
'H50	C_L = 25 pF, R_L = 280 Ω, C = 15 pF (GND to $\overline{X}$ of 'H50, 'H53, or 'H55; or to X of 'H52)	11		7.4	
'H52		14.8		9.8	
'H53		11.4		7.4	
'H55		11.4		7.7	

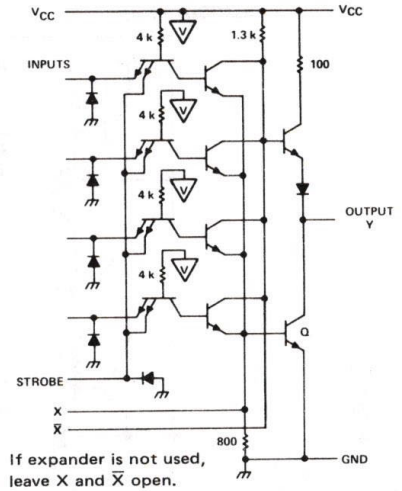
#Load circuit and voltage waveforms are shown on page 3-10.

TYPICAL ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE



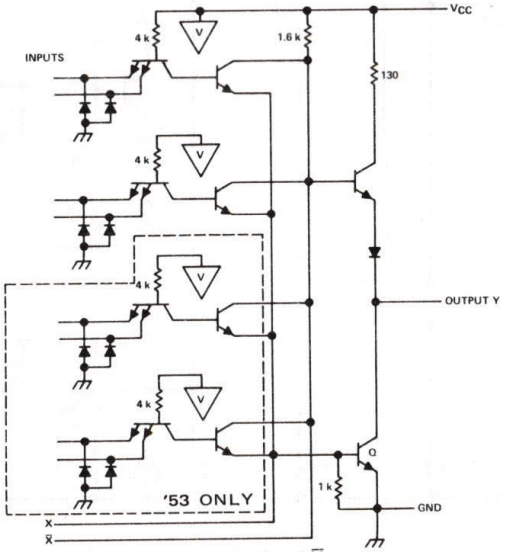


schematics (each gate)



If expander is not used, leave X and $\overline{X}$ open.

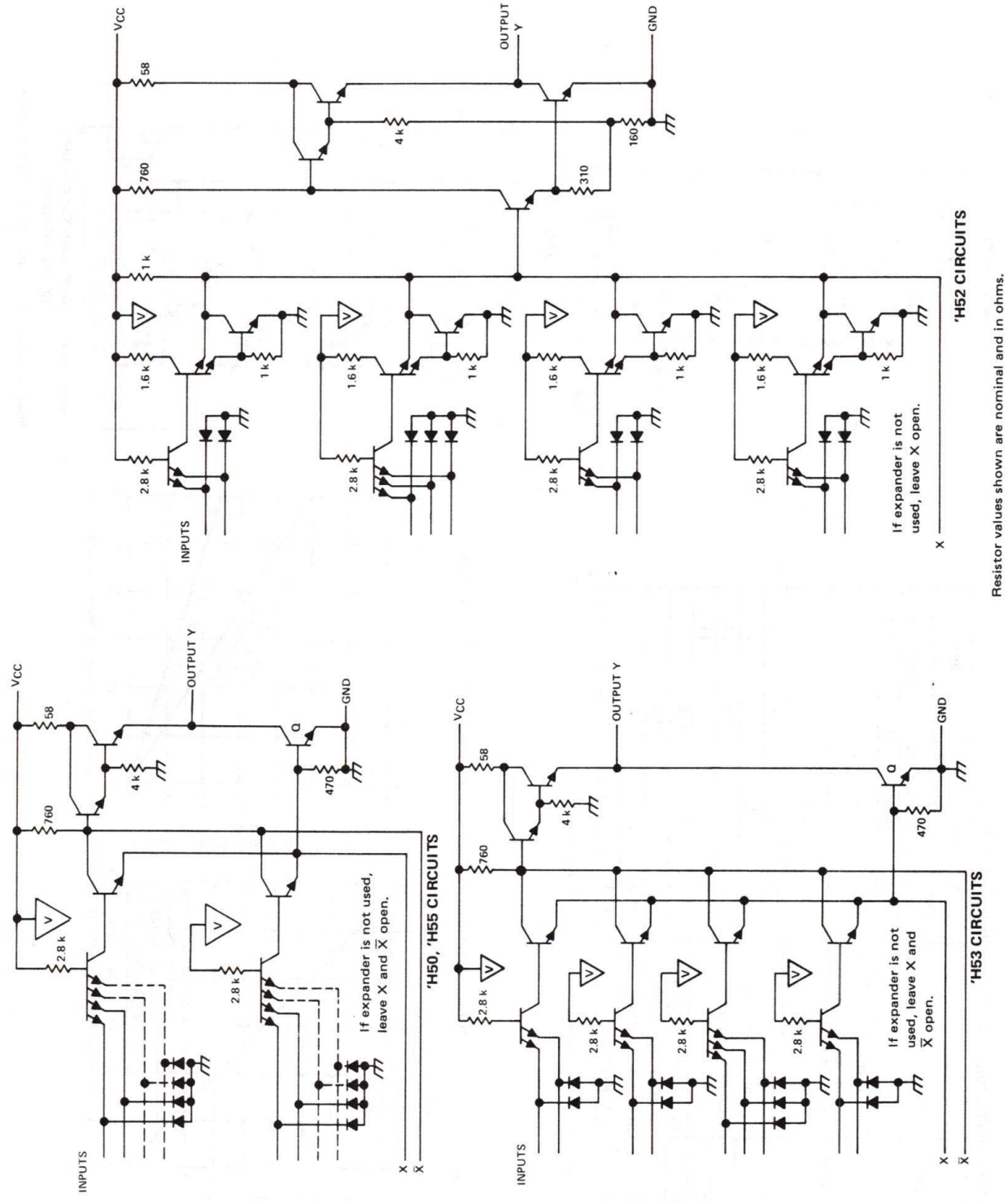
'23 CIRCUITS



If expander is not used, leave X and $\overline{X}$ open.

'50, '53 CIRCUITS

Resistor values shown are nominal and in ohms.



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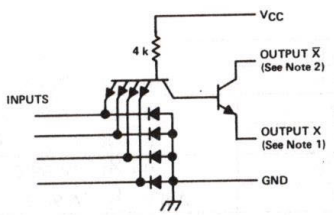
recommended operating conditions

	SN5460			SN7460			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

The '23, '50, and '53 are designed for use with up to four '60 expanders.

schematic (each gate)



'60 CIRCUITS

NOTES: 1. Connect to X input of '23, '50, or '53 circuit.
2. Connect to $\overline{X}$ input of '23, '50, or '53 circuit.

Resistor value shown is nominal and in ohms.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	SN5460 TEST CONDITIONS	SN5460 MIN	SN5460 TYP‡	SN5460 MAX	SN7460 TEST CONDITIONS	SN7460 MIN	SN7460 TYP‡	SN7460 MAX	UNIT
V_{IH}	High-level input voltage	15		2				2			V
V_{IL}	Low-level input voltage	16				0.8				0.8	V
$V_{\overline{X}X(on)}$	On-state voltage between expander outputs	15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1.1 V, $I_{\overline{X}}$ = 3.5 mA, T_A = −55°C			0.4	V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 3.8 mA, T_A = 0°C			0.4	V
$I_{X(on)}$	On-state expander current	15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1.1 V, $I_{\overline{X}}$ = 0, T_A = −55°C	−0.3			V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 0, T_A = 0°C	−0.43			mA
$I_{\overline{X}(off)}$	Off-state expander current	16	V_{CC} = 4.5 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 1.2 kΩ, T_A = −55°C			150	V_{CC} = 4.75 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 1.2 kΩ, T_A = 0°C			270	μA
I_I	Input current at maximum input voltage	4	V_{CC} = 5.5 V, V_I = 5.5 V			1	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	4	V_{CC} = 5.5 V, V_I = 2.4 V			40	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	5	V_{CC} = 5.5 V, V_I = 0.4 V			−1.6	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
$I_{CC(on)}$	Supply current, expander on	7	V_{CC} = 5.5 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0		1.2	2.5	V_{CC} = 5.25 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0		1.2	2.5	mA
$I_{CC(off)}$	Supply current, expander off	7	V_{CC} = 5.5 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0		2	4	V_{CC} = 5.25 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0		2	4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

recommended operating conditions

	SN54H60 SN54H62			SN74H60 SN74H62			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

See schematics next page

The 'H50, 'H53, and 'H55 are designed for use with up to four 'H60 expanders or one 'H62 expander.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	SN54H60, SN54H62 TEST CONDITIONS	MIN	TYP‡	MAX	SN74H60, SN74H62 TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		15		2				2			V
V_{IL}	Low-level input voltage		16				0.8				0.8	V
$V_{\overline{X}X(on)}$	On-state voltage between expander outputs		15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1.1 V, $I_{\overline{X}}$ = 5.85 mA, T_A = −55°C			0.4	V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 6.3 mA, T_A = 0°C			0.4	V
				V_{CC} = 5.5 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 7.85 mA, T_A = 125°C			0.4	V_{CC} = 5.25 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 7.4 mA, T_A = 70°C			0.4	
$I_{X(on)}$	On-state expander current		15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1.1 V, $I_{\overline{X}}$ = 0, T_A = −55°C	−470			V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 0, T_A = 0°C	−600			μA
$I_{\overline{X}(off)}$	Off-state expander current		16	V_{CC} = 4.5 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 575 Ω, T_A = −55°C			320	V_{CC} = 4.75 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 575 Ω, T_A = 0°C			570	μA
I_I	Input current at maximum input voltage		4	V_{CC} = 5.5 V, V_I = 5.5 V			1	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current		4	V_{CC} = 5.5 V, V_I = 2.4 V			50	V_{CC} = 5.25 V, V_I = 2.4 V			50	μA
I_{IL}	Low-level input current		5	V_{CC} = 5.5 V, V_I = 0.4 V			−2	V_{CC} = 5.25 V, V_I = 0.4 V			−2	mA
$I_{CC(on)}$	Supply current, expander on	'H60	7	V_{CC} = 5.5 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0,	1.9		3.5	V_{CC} = 5.25 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0	1.9		3.5	mA
		'H62			3.8		7		3.8		7	
$I_{CC(off)}$	Supply current, expander off	'H60	7	V_{CC} = 5.5 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0	3		4.5	V_{CC} = 5.25 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0	3		4.5	mA
		'H62			6		9		6		9	
$C_{\overline{X}}$	Expander output capacitance	'H60		V_{CC}, inputs, and X open; f = 1 MHz	5.4			V_{CC}, inputs, and X open; f = 1 MHz	5.4			pF
		'H62			6.0				6.0			

‡All typical values are at V_{CC} = 5 V (except $C_{\overline{X}}$), T_A = 25°C.

recommended operating conditions

	SN54H61			SN74H61			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

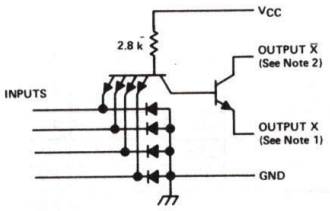
The 'H52 is designed for use with up to six 'H61 expanders.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

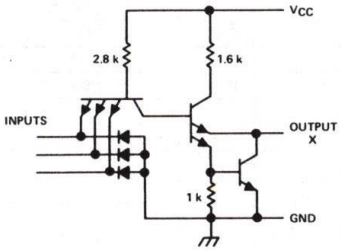
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	17		2			V
V_{IL}	Low-level input voltage	18				0.8	V
$V_{X(on)}$	On-state expander-output voltage	17	V_{CC} = MIN, V_{IH} = 2 V, I_X = 4.5 mA for SN54H61, 5.35 mA for SN74H61, T_A = MIN			1	V
$I_{X(off)}$	Off-state expander current	18	V_{CC} = MIN, V_{IL} = 0.8 V, V_X = 2.2 V, T_A = MAX			50	μA
I_I	Input current at maximum input voltage	4	V_{CC} = 5.5 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	4	V_{CC} = 5.5 V, V_I = 2.4 V			50	μA
I_{IL}	Low-level input current	5	V_{CC} = 5.5 V, V_I = 0.4 V			−2	mA
$I_{CC(on)}$	Supply current, expander on	7	V_{CC} = 5.5 V, V_I = 4.5 V		11	16	mA
$I_{CC(off)}$	Supply current, expander off	7	V_{CC} = 5.5 V, V_I = 0		5	7	mA
C_X	Expander output capacitance		V_{CC} and inputs open, f = 1 MHz		5.4		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V (except C_X), T_A = 25°C.

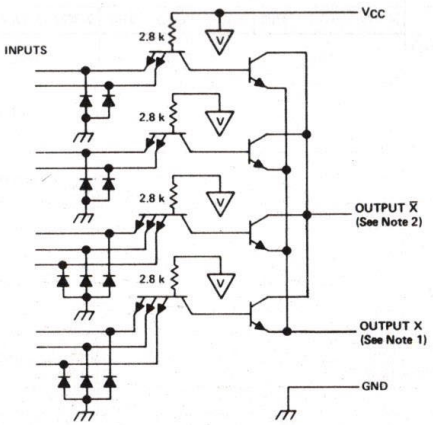
schematics (each gate)



'H60 CIRCUITS



'H61 CIRCUITS



'H62 CIRCUITS

NOTES: 1. Connect to X input of 'H50, 'H53, or 'H55 circuit.
2. Connect to X̄ input of 'H50, 'H53, or 'H55 circuit.

Resistor values shown are nominal and in ohms.

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recommended operating conditions

		SERIES 54/74	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−400			−400			−800			−800			−800	μA
Low-level output current, I_{OL}					16			16			16			16			16			16	mA
Pulse width, t_w	Clock high		20			20			30			20			25			25			ns
	Clock low		30			47			37			20			25			25			
	Preset or clear low		25			25			30			20			25			25			
Input setup time, t_{su}			20↑			0↑			20↑			10↑			20↑			0↑			ns
Input hold time, t_h			5↑			0↓			5↑			6↑			5↑			30↑			ns
Operating free-air temperature, T_A		Series 54	−55		125	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		Series 74	0		70	0		70	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8			0.8			0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5			−1.5			−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1			1			1	mA
I_{IH}	High-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX, V_I = 2.4 V			40			40			40			40			40			40	μA
		Clear				80			80			120			160			160			80	
		Preset				80			80			80			80			160			80	
		Clock				40			80			80			80			40			120	
I_{IL}	Low-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6			−1.6			−1.6			−1.6			−1.6	mA
		Clear ★				−3.2			−3.2			−3.2			−4.8			−3.2			−3.2	
		Preset ★				−3.2			−3.2			−1.6			−3.2			−3.2			−3.2	
		Clock				−1.6			−3.2			−3.2			−3.2			−1.6			−4.8	
I_{OS}	Short-circuit output current◆	Series 54	V_{CC} = MAX	−20		−57	−20		−57	−20		−57	−30		−85	−20		−57	−20		−57	mA
		Series 74		−18		−57	−18		−57	−18		−57	−30		−85	−18		−57	−18		−57	
I_{CC}	Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1		13	26		10	20		8.5	15		9	15		20	34		14	20.5	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
◆Not more than one output should be shorted at a time.
★Clear is tested with preset high and preset is tested with clear high.

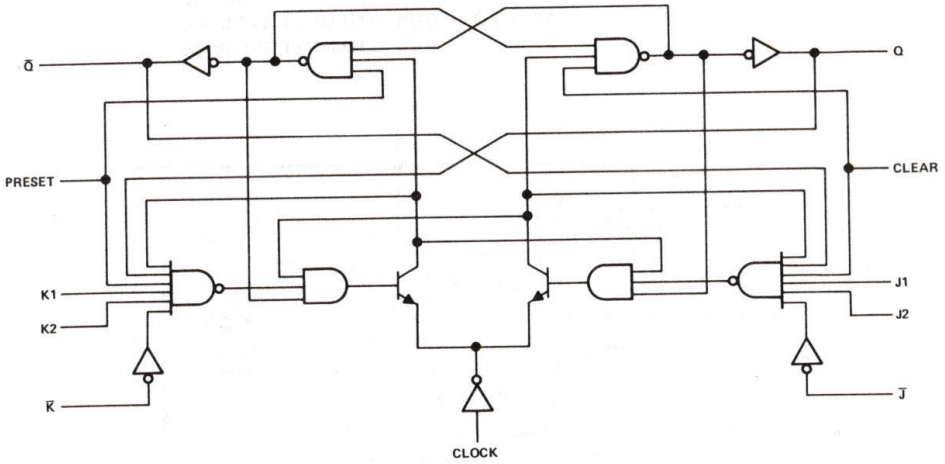
NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5 V for the '70, '110, and '111; and is grounded for all the others.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

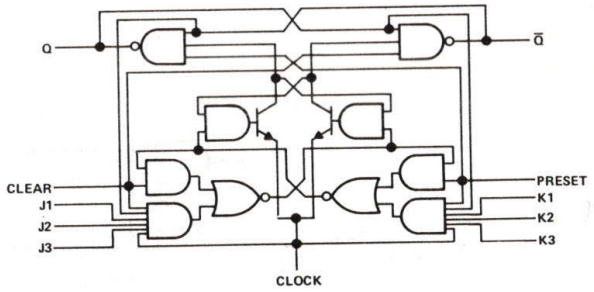
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'70			'72, '73 '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}				20	35		15	20		15	25		25	33		20	25		20	25		MHz
t_{PLH}	Preset (as applicable)	Q	C_L = 15 pF, R_L = 400 Ω, See Note 2			50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		$\overline{Q}$				50		25	40			40		23	35		18	25		21	30	
t_{PLH}	Clear (as applicable)	$\overline{Q}$				50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		Q				50		25	40			40		17	25		18	25		21	30	
t_{PLH}	Clock	Q or $\overline{Q}$			27	50		16	25		14	25		10	16		20	30		12	17	ns
t_{PHL}					18	50		25	40		20	40		18	28		13	20		20	30	

¶f_{max} ≡ maximum clock frequency; t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagrams



'70—GATED J-K WITH CLEAR AND PRESET

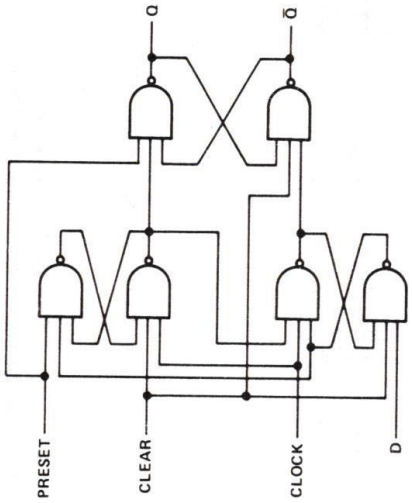


'72—GATED J-K WITH CLEAR AND PRESET

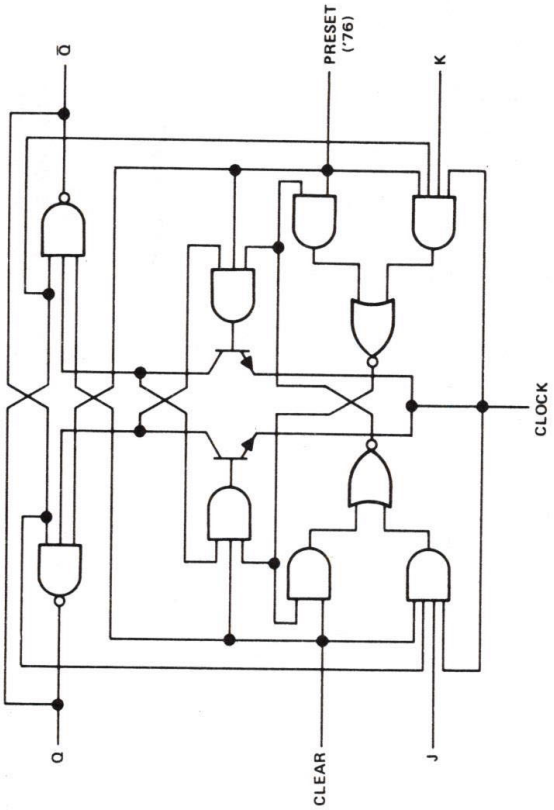
See following pages for:
'73—DUAL J-K WITH CLEAR
'74—DUAL D WITH CLEAR AND PRESET
'76—DUAL J-K WITH CLEAR AND PRESET
'107—DUAL J-K WITH CLEAR

'109—DUAL J-$\overline{K}$ WITH CLEAR AND PRESET
'110—GATED J-K WITH CLEAR AND PRESET
'111—DUAL J-K WITH CLEAR AND PRESET

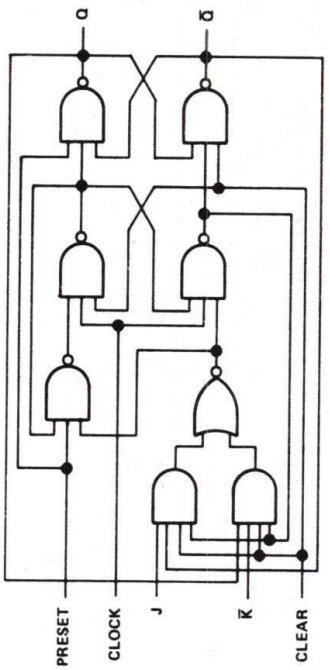
functional block diagrams (continued)



'74—DUAL D WITH CLEAR AND PRESET



'73—DUAL J-K WITH CLEAR
'76—DUAL J-K WITH CLEAR AND PRESET
'107—DUAL J-K WITH CLEAR



'109—DUAL J-K̄ WITH CLEAR AND PRESET

functional block diagrams (continued)

'111—DUAL J-K WITH CLEAR AND PRESET

'110—GATED J-K WITH CLEAR AND PRESET

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−3.2 mA	2 kΩ
−4.8 mA	1.3 kΩ

TYPICAL OF ALL OUTPUTS

recommended operating conditions

		SERIES 54H/74H	'H71			'H72, 'H73, 'H76			'H74			'H78			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54H	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74H	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−500			−500			−1000			−500	μA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		12			12			15			12			ns
	Clock low		28			28			13.5			28			
	Clear or preset low		16			16			25			16			
Setup time, t_{su}	High-level data		0↑			0↑			10↑			0↑			ns
	Low-level data		0↑			0↑			15↑			0↑			
Hold time, t_h			0↓			0↓			5↑			0↓			ns
Operating free-air temperature, T_A		Series 54H	−55		125	−55		125	−55		125	−55		125	°C
		Series 74H	0		70	0		70	0		70	0		70	

↓↑ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'H71			'H72, 'H73, 'H76			'H74			'H78			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			2			2			V
V_{IL} Low-level input voltage						0.8			0.8			0.8			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −8 mA				−1.5			−1.5			−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1			1			1	mA
I_{IH} High-level input current	D, J, or K	V_{CC} = MAX, V_I = 2.4 V				50			50			50			50	μA
	Clear								100			150			200	
	Preset					150			100			100			100	
	Clock					100			50			100			100	
I_{IL} Low-level input current	D, J, or K	V_{CC} = MAX, V_I = 0.4 V				−2			−2			−2			−2	mA
	Clear ★								−4			−4			−8	
	Preset ★					−6			−4			−2			−4	
	Clock					−4			−2			−4			−4	
I_{OS} Short-circuit output current◆		V_{CC} = MAX		−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC} Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1	Series 54H		19	30		16	25		15	21		16	25	mA
			Series 74H		19	30		16	25		15	25		16	25	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
◆Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
★Clear is tested with preset high and preset is tested with clear high.
NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'H71, 'H72, 'H73, 'H76, 'H78			'H74			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 25 pF, R_L = 280 Ω, See Note 2	25	30		35	43		MHz
t_{PLH}	Preset (as applicable)	Q			6	13			20	ns
t_{PHL}		$\overline{Q}$			12	24			30	
t_{PLH}	Clear (as applicable)	$\overline{Q}$			6	13			20	ns
t_{PHL}		Q			12	24			30	
t_{PLH}	Clock	Q or $\overline{Q}$			14	21		8.5	15	ns
t_{PHL}					22	27		13	20	

¶ f_{max} ≡ maximum clock frequency; t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

schematics of input and outputs

EQUIVALENT OF EACH INPUT

I_{IL} MAX	R_{eq} NOM
−2 mA	2.8 kΩ
−4 mA	1.4 kΩ
−6 mA	933 Ω
−8 mA	700 Ω

TYPICAL OF ALL OUTPUTS

functional block diagrams

'H71—GATED J-K WITH PRESET

'H72—GATED J-K WITH CLEAR AND PRESET

Same functional block diagram as for '74, see page 6-48.

'H74—DUAL D WITH CLEAR AND PRESET

'H73—DUAL J-K WITH CLEAR
'H76—DUAL J-K WITH CLEAR AND PRESET
'H78—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

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recommended operating conditions

		SERIES 54H/74H	'H101			'H102, 'H106			'H103			'H108			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54H	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74H	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−500			−500			−500			−500	μA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		10			10			10			10			ns
	Clock low		15			15			15			15			
	Clear or preset low		16			16			16			16			
Setup time, t_{su}	High-level data		10↓			10↓			10↓			10↓			ns
	Low-level data		13↓			13↓			13↓			13↓			
Hold time, t_h			0↓			0↓			0↓			0↓			ns
Operating free-air temperature, T_A		Series 54H	−55		125	−55		125	−55		125	−55		125	°C
		Series 74H	0		70	0		70	0		70	0		70	

↓The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'H101			'H102, 'H106			'H103			'H108			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			2			2			V
V_{IL} Low-level input voltage					0.8			0.8			0.8			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5			−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −500 μA	2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1	mA
I_{IH} High-level input current	Any J or K	V_{CC} = MAX, V_I = 2.4 V			50			50			50			50	μA
	Clear							100			100			200	
	Preset				100			100						100	
	Clock		0		−1	0		−1	0		−1	0		−1	mA
I_{IL} Low-level input current	Any J or K	V_{CC} = MAX, V_I = 0.4 V		−1	−2		−1	−2		−1	−2		−1	−2	mA
	Clear						−1	−2		−1	−2		−2	−4	
	Preset			−1	−2		−1	−2					−1	−2	
	Clock			−3	−4.8		−3	−4.8		−3	−4.8		−6	−9.6	
I_{OS} Short-circuit output current◆		V_{CC} = MAX	−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC} Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1		20	38		20	38		20	38		20	38	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

◆Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

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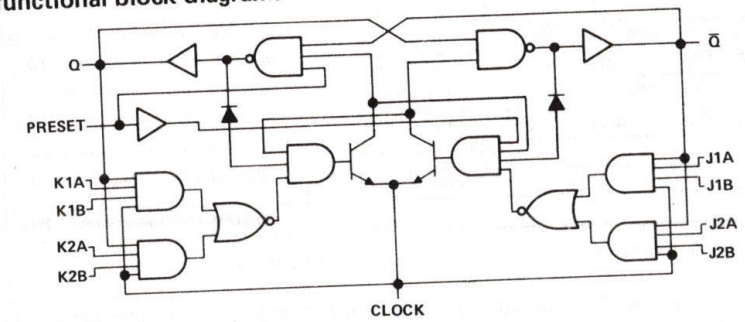
switching characteristics, V_{CC} = 5 V, T_A = 25°C

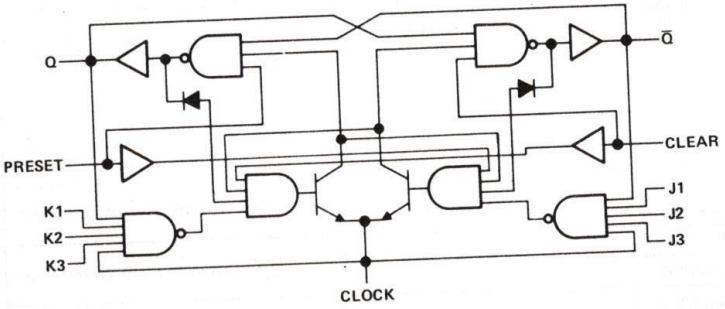
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 25 pF, R_L = 280 Ω, See Note 2	40	50		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$			8	12	ns
t_{PHL}	Preset or clear (clock high)	$\overline{Q}$ or Q			15	20	ns
	Preset or clear (clock low)				23	35	
t_{PLH}	Clock	Q or $\overline{Q}$			10	15	ns
t_{PHL}					16	20	

¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagrams

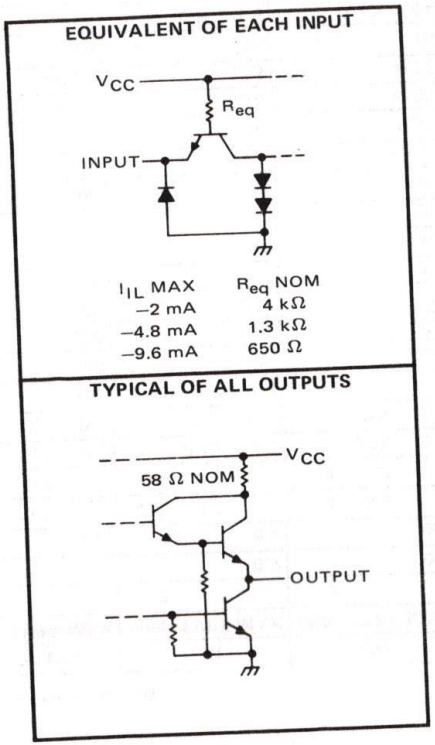


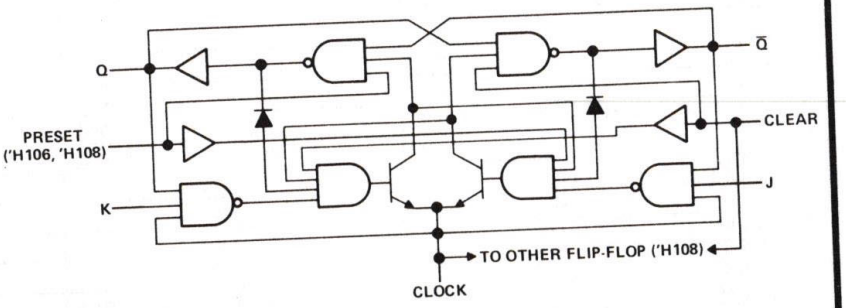
'H101—GATED J-K WITH PRESET



'H102—GATED J-K WITH CLEAR AND PRESET

schematics of inputs and outputs





'H103—DUAL J-K WITH CLEAR
'H106—DUAL J-K WITH CLEAR AND PRESET
'H108—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

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recommended operating conditions

		SERIES 54L/74L	'L71			'L72, 'L73			'L74			'L78			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54L	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74L	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}		Series 54L			−100			−100			−100			−100	μA
		Series 74L			−200			−200			−200			−200	
Low-level output current, I_{OL}		Series 54L			2			2			2			2	mA
		Series 74L			3.6			3.6			3.6			3.6	
Pulse width, t_w	Clock high		200			200			200			200			ns
	Clock low		200			200			200			200			
	Clear or preset low		100			100			100			100			
Setup time, t_{su}			0↑			0↑			50↑			0↑			ns
Hold time, t_h			0↓			0↓			15↑			0↓			ns
Operating free-air temperature, T_A		Series 54L	−55		125	−55		125	−55		125	−55		125	°C
		Series 74L	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'L71			'L72, 'L73			'L74			'L78			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			2			2			V
V_{IL} Low-level input voltage	Clock input				0.6			0.6			0.7			0.6	V
	All other inputs				0.7			0.7			0.7			0.7	
V_{OH} High-level output voltage	Series 54L	V_{CC} = MIN, V_{IH} = 2 V,	2.4	3.3		2.4	3.3		2.4	3.3		2.4	3.3		V
	Series 74L	V_{IL} = V_{IL} max, I_{OH} = MAX	2.4	3.2		2.4	3.2		2.4	3.2		2.4	3.2		
V_{OL} Low-level output voltage	Series 54L	V_{CC} = MIN, V_{IH} = 2 V,		0.15	0.3		0.15	0.3		0.15	0.3		0.15	0.3	V
	Series 74L	V_{IL} = V_{IL} max, I_{OL} = MAX		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	
I_I Input current at maximum input voltage	R, S, J, K, or D	V_{CC} = MAX, V_I = 5.5 V			100			100			100			100	μA
	Clear				200			200			300			400	
	Preset				200			200			200			200	
	Clock				200			200			200			400	
I_{IH} High-level input current	R, S, J, K, or D	V_{CC} = MAX, V_I = 2.4 V			10			10			10			10	μA
	Clear				20			20			30			40	
	Preset				20			20			20			20	
	Clock				−200			−200			20			−400	
I_{IL} Low-level input current	R, S, J, K, or D	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18			−0.18			−0.18	mA
	Clear				−0.36			−0.36			−0.36			−0.72	
	Preset				−0.36			−0.36			−0.18			−0.36	
	Clock				−0.36			−0.36			−0.36			−0.72	
I_{OS} Short-circuit output current		V_{CC} = MAX	−3		−15	−3		−15	−3		−15	−3		−15	mA
I_{CC} Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1		0.76	1.44		0.76	1.44		0.8	1.5		0.76	1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

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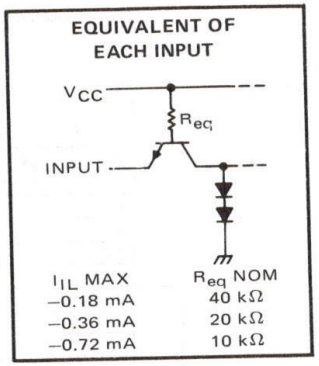
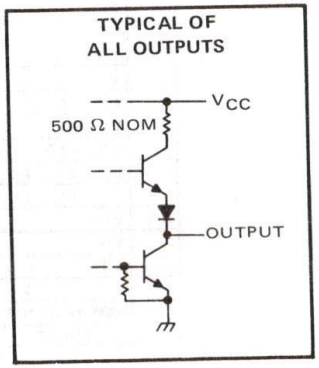
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'L71, 'L72, 'L73, 'L78			'L74			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 50 pF, R_L = 4 kΩ, See Note 2	2.5	3		2.5	3		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$			35	75		50	75	ns
t_{PHL}	Preset or clear (clock high)	$\overline{Q}$ or Q			60	150		80	150	ns
	Preset or clear (clock low)					200		80	150	
t_{PLH}	Clock	Q or $\overline{Q}$		10	35	75	15	65	100	ns
t_{PHL}				10	60	150	15	65	150	

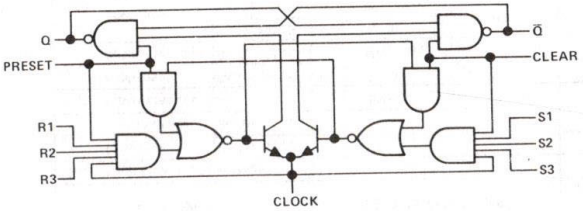
¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

schematics of inputs and outputs

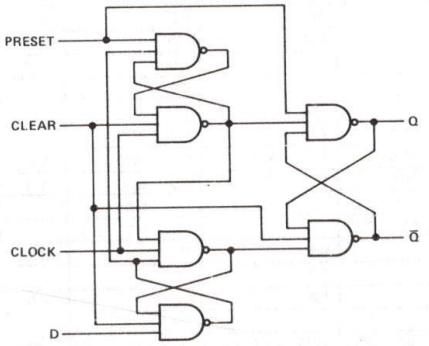




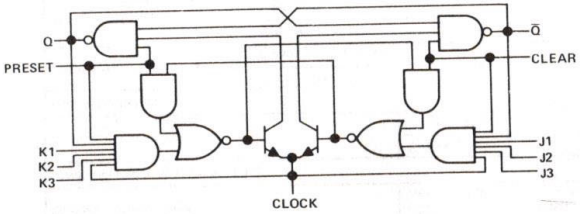
functional block diagrams



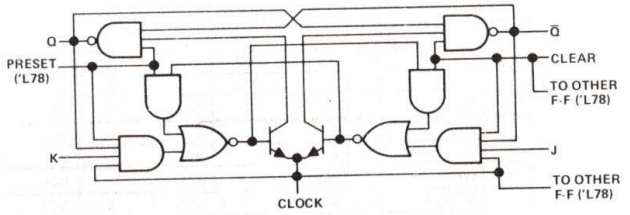
'L71—GATED R-S WITH CLEAR AND PRESET



'L74—DUAL D WITH CLEAR AND PRESET



'L72—GATED J-K WITH CLEAR AND PRESET



'L73—DUAL J-K WITH CLEAR
'L78—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

		SERIES 54LS/74LS	'LS73A, 'LS107A, 'LS113A			'LS74A			'LS76A, 'LS112A			'LS78A, 'LS114A			'LS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54LS	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74LS	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−400			−400			−400			−400	μA
Low-level output current, I_{OL}		Series 54LS			4			4			4			4			4	mA
		Series 74LS			8			8			8			8			8	
Clock frequency, f_{clock}			0		30	0		25	0		30	0		30	0		25	MHz
Pulse width, t_w	Clock high		20			25			20			20			25			ns
	Preset or clear low		25			25			25			25			25			
Setup time, t_{su}	High-level data		20↓			20↑			20↓			20↓			35↑			ns
	Low-level data		20↓			20↑			20↓			20↓			25↑			
Hold time, t_h			0↓			5↑			0↓			0↓			5↑			ns
Operating free-air temperature, T_A		Series 54LS	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		Series 74LS	0		70	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'LS73A, 'LS107A, 'LS113A			'LS74A			'LS76A, 'LS112A			'LS78A, 'LS114A			'LS109A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			2			2			V
V_{IL}	Low-level input voltage	Series 54LS					0.7			0.7			0.7			0.7			0.7	V
		Series 74LS					0.8			0.8			0.8			0.8			0.8	
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5			−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage	Series 54LS	V_{CC} = MIN,	V_{IH} = 2 V,	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		V
		Series 74LS	V_{IL} = V_{IL} max,	I_{OH} = −400 μA	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Series 54LS	V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4	V
		Series 74LS	V_{IL} = V_{IL} max,			0.35	0.5		0.35	0.5		0.35	0.5		0.35	0.5		0.35	0.5	
		Series 74LS	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4	
I_I	Input current at maximum input voltage	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 7 V			0.1			0.1			0.1			0.1			0.1	mA
		Clear					0.3			0.2			0.3			0.6			0.2	
		Preset					0.3			0.2			0.3			0.3			0.2	
		Clock					0.4			0.1			0.4			0.8			0.1	
I_{IH}	High-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 2.7 V			20			20			20			20			20	μA
		Clear					60			40			60			120			40	
		Preset					60			40			60			60			40	
		Clock					80			20			80			160			20	
I_{IL}	Low-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4			−0.4			−0.4			−0.4	mA
		Clear					−0.8			−0.8			−0.8			−1.6			−0.8	
		Preset					−0.8			−0.8			−0.8			−0.8			−0.8	
		Clock					−0.8			−0.4			−0.8			−1.6			−0.4	
I_{OS}	Short-circuit output current♦	Series 54LS	V_{CC} = MAX,	See Note 1	−20		−100	−20		−100	−20		−100	−20		−100	−20		−100	mA
		Series 74LS			−20		−100	−20		−100	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current (Total)		V_{CC} = MAX,	See Note 2		4	6		4	8		4	6		4	6		4	8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

NOTES: 1. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.
2. With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

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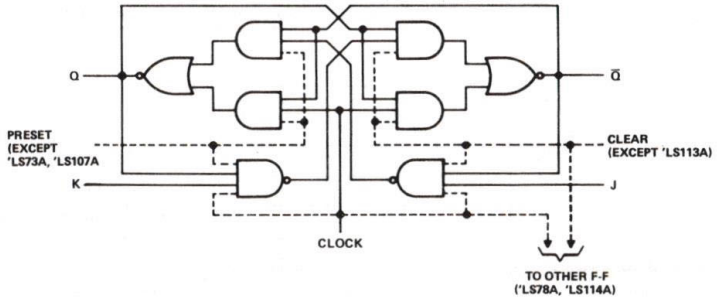
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS73A,'LS76A,'LS78A, 'LS107A,'LS112A, 'LS113A,'LS114A			'LS74A, 'LS109A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF,	30	45		25	33		MHz
t_{PLH}	Clear, preset, or clock (as appropriate)	Q or $\overline{Q}$	R_L = 2 kΩ,		15	20		13	25	ns
t_{PHL}			See Note 2		15	20		25	40	ns

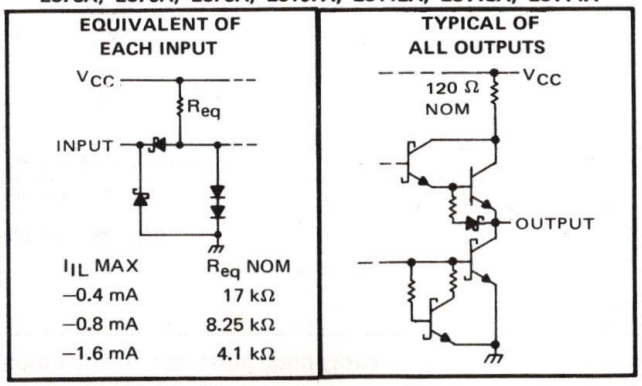
¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

functional block diagrams and schematics of inputs and outputs

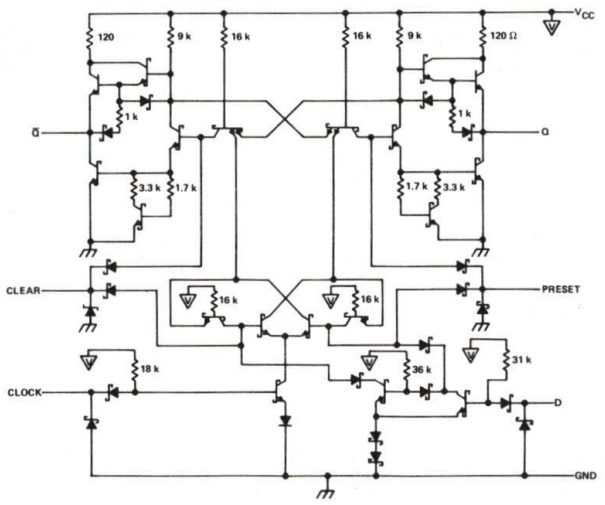


'LS73A, 'LS107A—DUAL J-K WITH CLEAR
'LS76A, 'LS112A—DUAL J-K WITH CLEAR AND PRESET
'LS78A, 'LS114A—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK
'LS113A—DUAL J-K WITH PRESET

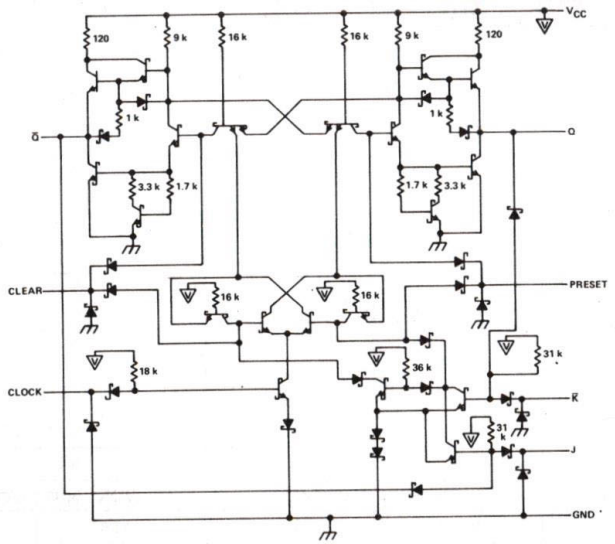
'LS73A, 'LS76A, 'LS78A, 'LS107A, 'LS112A, 'LS113A, 'LS114A



schematics of 'LS74A and 'LS109A



'LS74A—DUAL D WITH CLEAR AND PRESET



'LS109A—DUAL J-$\overline{K}$ WITH CLEAR AND PRESET

recommended operating conditions

		SERIES 54S/74S	'S74			'S112			'S113			'S114			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−1			−1			−1			−1	mA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		6			6			6			6			ns
	Clock low		7.3			6.5			6.5			6.5			
	Clear or preset low		7			8			8			8			
Input setup time, t_{su}	High-level data		3↑			3↓			3↓			3↓			ns
	Low-level data		3↑			3↓			3↓			3↓			
Input hold time, t_h			2↑			0↓			0↓			0↓			ns
Operating free-air temperature, T_A		Series 54S	−55		125	−55		125	−55		125	−55		125	°C
		Series 74S	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'S74			'S112			'S113			'S114			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	Series 54S	V_{CC} = MIN, V_{IH} = 2 V,	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		V
		Series 74S	V_{IL} = 0.8 V, I_{OH} = −1 mA	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1	mA
I_{IH}	High-level input current	J, K, or D	V_{CC} = MAX, V_I = 2.7 V			50			50			50			50	μA
		Clear				150			100						200	
		Preset				100			100			100			100	
		Clock				100			100			100			200	
I_{IL}	Low-level input current	J, K, or D	V_{CC} = MAX, V_I = 0.5 V			−2			−1.6			−1.6			−1.6	mA
		Clear ★				−6			−7						−14	
		Preset ★				−4			−7			−7			−7	
		Clock				−4			−4			−4			−8	
I_{OS}	Short-circuit output current◆		V_{CC} = MAX	−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC}	Supply current (average per flip-flop)		V_{CC} = MAX, See Note 1		15	25		15	25		15	25		15	25	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

◆Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

★Clear is tested with preset high and preset is tested with clear high.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

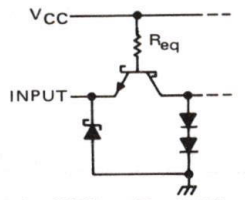
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S74			'S112, 'S113, 'S114			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Note 2	75	110		80	125		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$			4	6		4	7	ns
t_{PHL}	Preset or clear (clock high)	$\overline{Q}$ or Q			9	13.5		5	7	ns
	Preset or clear (clock low)				5	8		5	7	
t_{PLH}	Clock	Q or $\overline{Q}$			6	9		4	7	ns
t_{PHL}					6	9		5	7	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

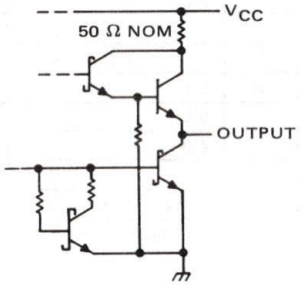
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

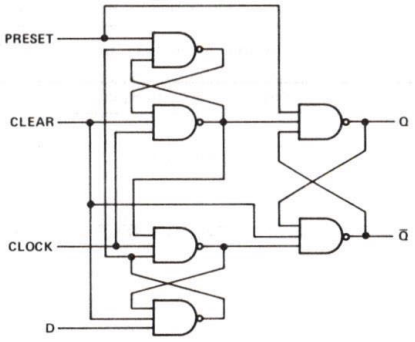


I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−2 mA	2.8 kΩ
−4 mA	1.4 kΩ
−6 mA	940 Ω
−7 mA	900 Ω
−8 mA	700 Ω
−14 mA	450 Ω

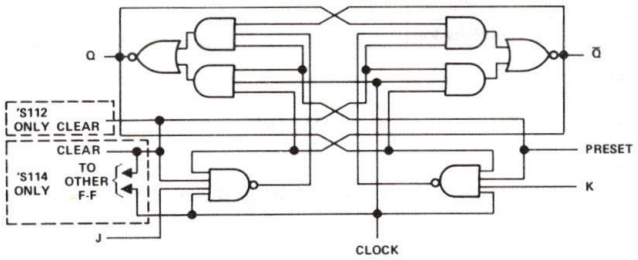
TYPICAL OF ALL OUTPUTS



functional block diagrams



'S74—DUAL D WITH CLEAR AND PRESET



'S112—DUAL J-K WITH CLEAR AND PRESET
'S113—DUAL J-K WITH PRESET
'S114—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

	54 FAMILY / 74 FAMILY	SN54279 / SN74279			SN54LS279 / SN74LS279			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				−800			−400	μA
Low-level output current, I_{OL}	54 Family			16			4	mA
	74 Family			16			8	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	°C
	74 Family	0		70	0		70	

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54279 / SN74279			SN54LS279 / SN74LS279			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level output voltage				2			2			V
V_{IL}	Low-level output voltage			54 Family			0.8			0.7	V
				74 Family			0.8			0.8	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = §					−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = MAX		54 Family	2.4	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4	V
				74 Family		0.2	0.4		0.35	0.5	
			I_{OL} = 4 mA	Series 74LS					0.35	0.4	
I_I	Input current at maximum input voltage	V_{CC} = MAX		V_I = 5.5 V			1				mA
				V_I = 7 V						0.1	
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4 V			40				μA
				V_I = 2.7 V						20	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V					−1.6			−0.4	mA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX		54 Family	−18		−55	−20		−100	mA
				74 Family	−18		−57	−20		−100	
I_{CC}	Supply current	V_{CC} = MAX, See note 1				18	30		3.8	7	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS'.

♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS', duration of the output short circuit should not exceed one second.

NOTE 1: I_{CC} is measured with all $\overline{R}$ inputs grounded, all $\overline{S}$ inputs at 4.5 V, and all outputs open.

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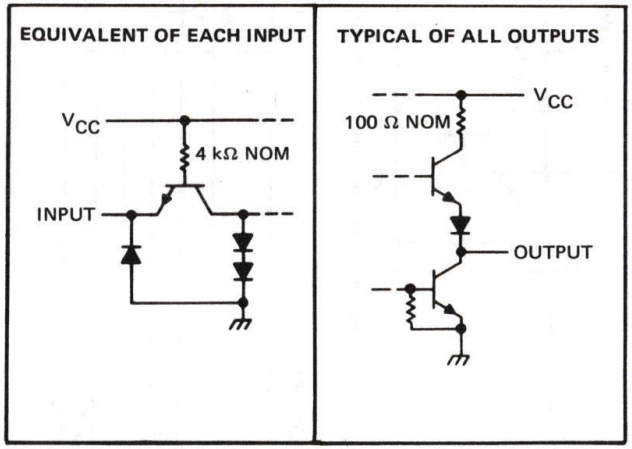
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'279			'LS279			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{S}$ input	C_L = 15 pF, See Notes 2 and 3		12	22		12	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{S}$ input			9	15		13	21	
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{R}$ input			15	27		15	27	

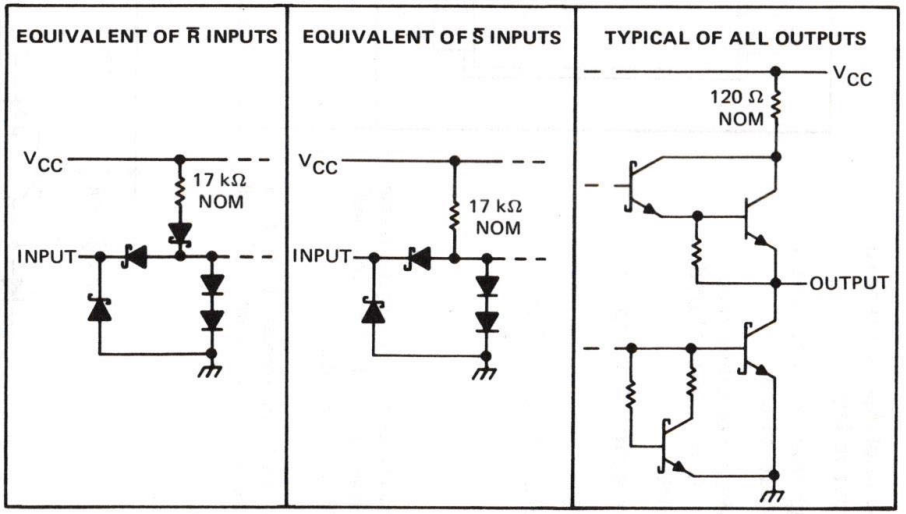
NOTE 2: Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.
NOTE 3: R_L = 400 Ω for '279, R_L = 2 kΩ for 'LS279.

schematics of inputs and outputs

'279 CIRCUITS



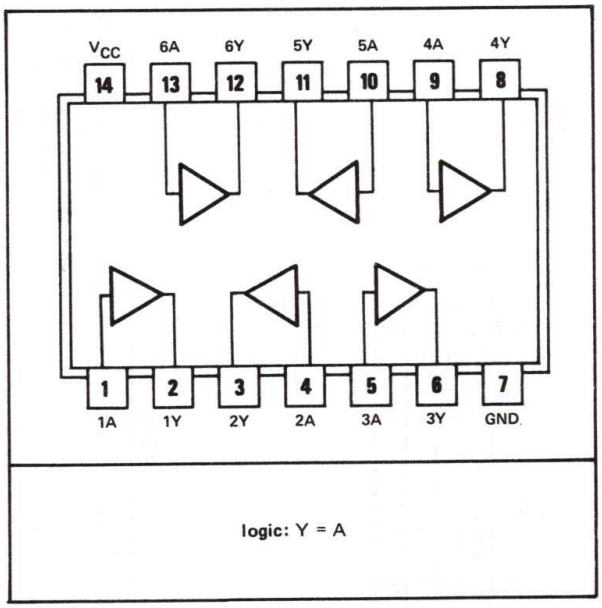
'LS279 CIRCUITS



SN54LS63, SN74LS63
HEX CURRENT-SENSING INTERFACE GATES WITH TOTEM-POLE OUTPUTS

- Translates low-level input current to low-level output voltage
- Translates high-level input current to high-level output voltage
- Interfaces to PLA's or other logic elements that source current but do not sink current
- Operates from a single 5 V supply
- TTL compatible
- Low power dissipation . . .40 mW typical

SN54LS63 . . . J OR W PACKAGE
SN74LS63 . . . J OR N PACKAGE



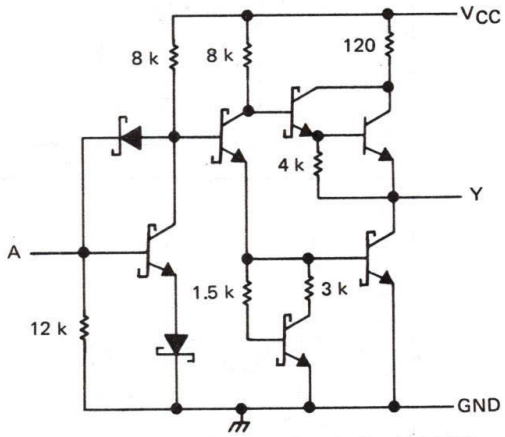
logic: Y = A

description

Each of these Schotty-clamped interface gates is able to discriminate between low-level ($\leqslant$ 50 μA) and high-level ($\geqslant$ 200 μA) input currents.

The outputs are fabricated with standard Low-Power Schottky design rules and are compatible with all TTL families.

schematic (each gate)



Resistor values shown are nominal and in ohms.

recommended operating conditions

	SN54LS63			SN74LS63			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Input current, I_I			1			1	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

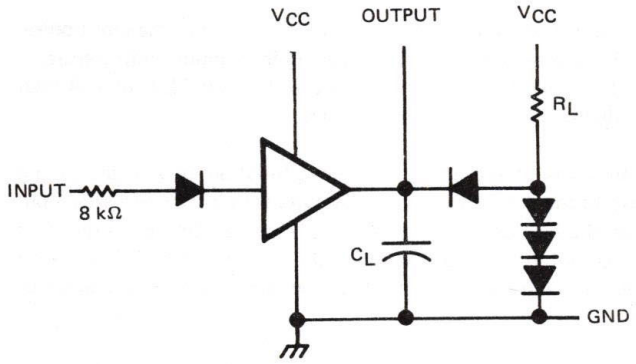
PARAMETER		TEST CONDITIONS†			SN54LS63			SN74LS63			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_I	Input voltage	I_I = 50 μA,	V_{CC} = MIN		0.35	1.05	1.75	0.6	1.05	1.6	V
		I_I = 200 μA,	V_{CC} = MAX		0.6	1.30	2	0.85	1.30	1.8	
V_{OH}	High-level output voltage	V_{CC} = MAX	I_I = 200 μA	I_{OH} = −400 μA,	3.5	3.4		3.2	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_I = 50 μA	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	I_I = 600 μA		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 1			8	16		8	16	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of output short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

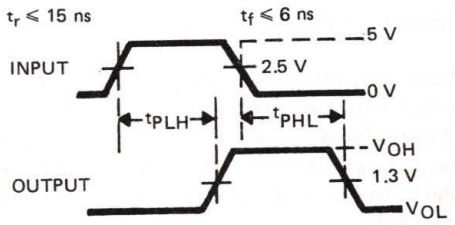
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propogation delay time, low-to-high-level output	C_L = 15 pF, R_L = 2 kΩ		27	45	ns
t_{PHL}	Propogation delay time, high-to-low-level output			15	25	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: a. C_L includes probe and jig capacitance
b. All diodes are 1N916 or 1N3064

TEST CIRCUIT



VOLTAGE WAVEFORMS

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TYPES SN54121, SN54L121, SN74121, SN74L121
MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

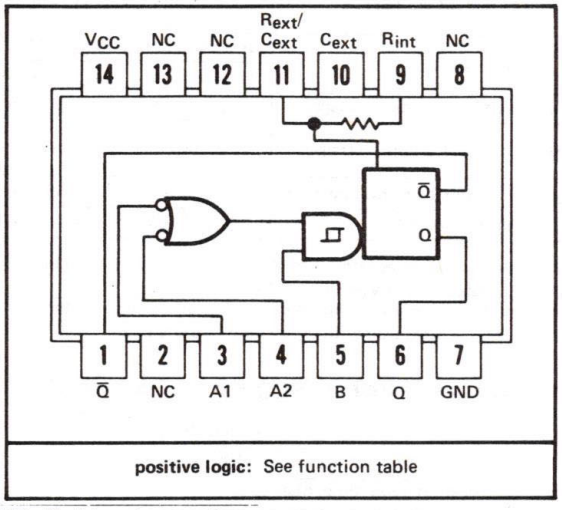
- Programmable Output Pulse Width
  With R_{int} . . . 35 ns Typ
  With R_{ext}/C_{ext} . . . 40 ns to 28 Seconds
- Internal Compensation for Virtual Temperature Independence
- Jitter-Free Operation up to 90% Duty Cycle
- Inhibit Capability

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎍
↓	H	H	⎍	⎍
↓	↓	H	⎍	⎍
L	X	↑	⎍	⎍
X	L	↑	⎍	⎍

For explanation of function table symbols, see page 3-8.

SN54121 . . . J OR W PACKAGE
SN54L121 . . . J OR T PACKAGE
SN74121, SN74L121 . . . J OR N PACKAGE



positive logic: See function table

NC—No internal connection

NOTES: 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext}.
2. To use the internal timing resistor, connect R_{int} to V_{CC}. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

description

6

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54121/SN54L121 and 2 kΩ to 40 kΩ for the SN74121/SN74L121). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_{ext}R_T\ln 2 \approx 0.7\ C_{ext}R_T$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

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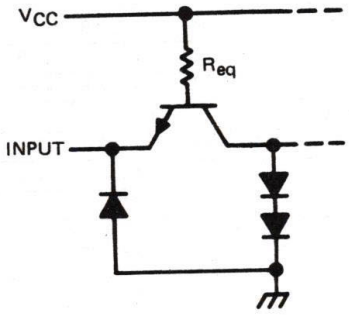
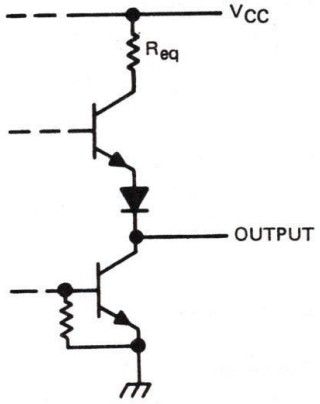
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM '121	R_{eq} NOM 'L121
A1	4 kΩ	8 kΩ
A2	4 kΩ	8 kΩ
B	2 kΩ	4 kΩ

TYPICAL OF BOTH OUTPUTS



'121: R_{eq} = 130 Ω NOM
'L121: R_{eq} = 260 Ω NOM

recommended operating conditions

		54 FAMILY 74 FAMILY	SN54121 SN74121			SN54L121 SN74L121			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−200	μA
Low-level output current, I_{OL}					16			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B		1			1			V/s
	Logic inputs, A1, A2		1			1			V/μs
Input pulse width, $t_{w(in)}$			50			100			ns
External timing resistance, R_{ext}		54 Family	1.4		30	1.4		30	kΩ
		74 Family	1.4		40	1.4		40	
External timing capacitance, C_{ext}			0		1000	0		1000	μF
Duty cycle	R_T = 2 kΩ				67			67	%
	R_T = MAX R_{ext}				90			90	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	°C
		74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54121 SN74121			SN54L121 SN74L121			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.4	2		1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.8	1.4		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2		1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		0.8	1.35		V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = MAX		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	A1 or A2			40			20	μA
			B			80			40	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	A1 or A2			−1.6			−0.8	mA
			B			−3.2			−1.6	
I_{OS}	Short-circuit output current♦	V_{CC} = MAX	54 Family	−20		−55	−10		−27	mA
			74 Family	−18		−55	−9		−27	
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		13	25		7	12	mA
			Triggered		23	40		9	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'121			'L121			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level Q output from either A input	C_L = 15 pF, R_L = 400 Ω for '121, R_L = 800 Ω for 'L121, See Note 3	C_{ext} = 80 pF, R_{int} to V_{CC}		45	70			140	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from B input				35	55			110	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output from either A input				50	80			160	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output from B input				40	65			130	ns
$t_{w(out)}$	Pulse width obtained using internal timing resistor		C_{ext} = 80 pF, R_{int} to V_{CC}	70	110	150	70	225	260	ns
$t_{w(out)}$	Pulse width obtained with zero timing capacitance		C_{ext} = 0, R_{int} to V_{CC}		30	50		35	70	ns
$t_{w(out)}$	Pulse width obtained using external timing resistor		C_{ext} = 100 pF, R_T = 10 kΩ	600	700	800	600	700	850	ns
			C_{ext} = 1 μF, R_T = 10 kΩ	6	7	8	6	7	8	ms

NOTE 3: Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS§

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

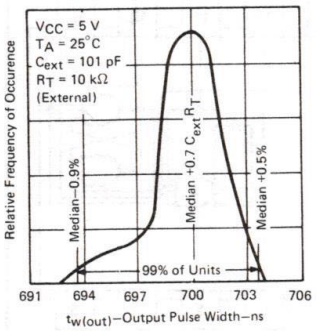


FIGURE 1

VARIATION IN INTERNAL TIMING RESISTOR VALUE
vs
FREE-AIR TEMPERATURE

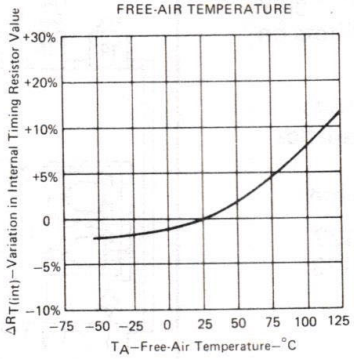


FIGURE 2

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

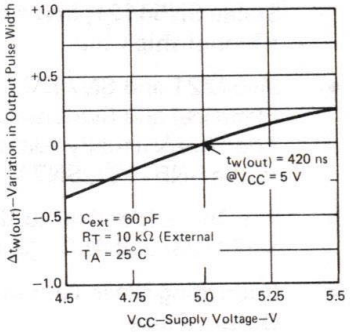


FIGURE 3

SCHMITT TRIGGER THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

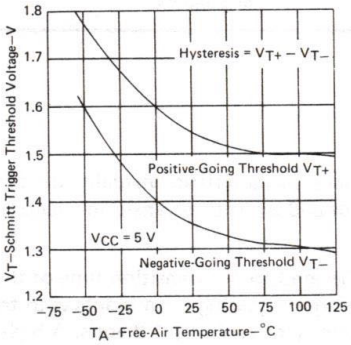


FIGURE 4

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

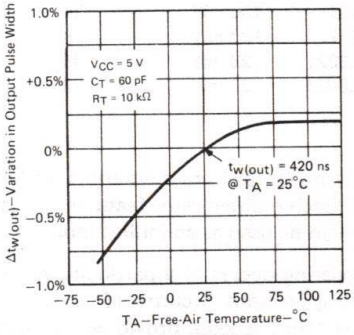


FIGURE 5

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

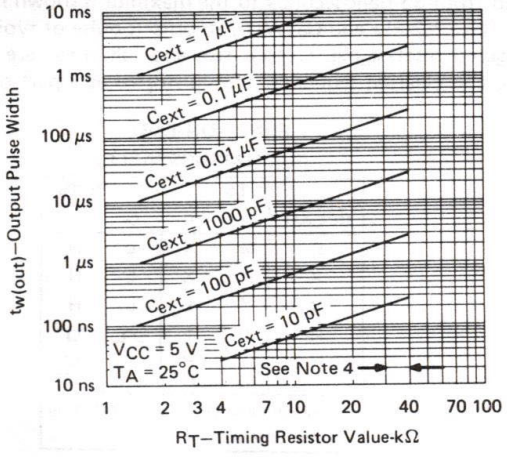


FIGURE 6

OUTPUT PULSE WIDTH
vs
EXTERNAL CAPACITANCE

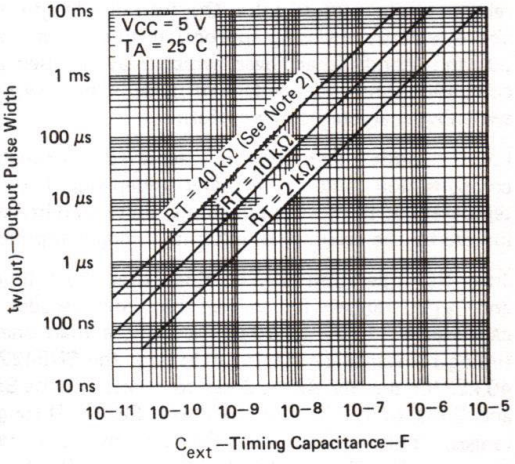


FIGURE 7

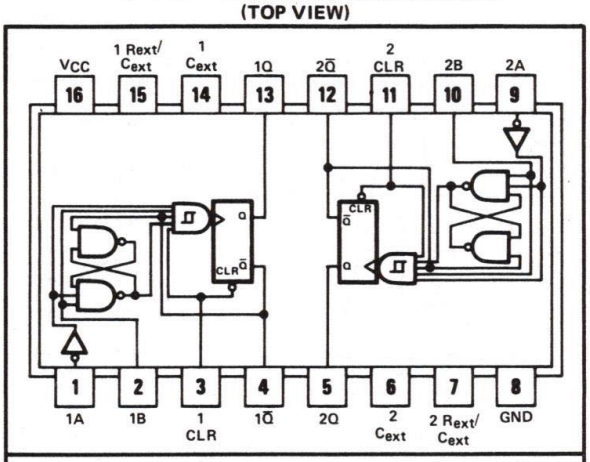
NOTE 4: These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54L121.
§ Data for temperatures below 0°C and above 70°C are applicable for SN54121 and SN54L121.

TYPES SN54221, SN54LS221, SN74221, SN74LS221
DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- **SN54221, SN54LS221, SN74221 and SN74LS221 Are Dual Versions of Highly Stable SN54121, SN74121 One-Shots on a Monolithic Chip**
- **SN54221 and SN74221 Demonstrate Electrical and Switching Characteristics That Are Virtually Identical to the SN54121, SN74121 One-Shots**
- **Pin-Out Is Identical to the SN54123 SN74123, SN54LS123, SN74LS123**
- **Overriding Clear Terminates Output Pulse**

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54221	130 mW	21 s
SN74221	130 mW	28 s
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

SN54221, SN54LS221 . . . J OR W PACKAGE
SN74221, SN74LS221 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: Low input to clear resets Q low and $\overline{Q}$ high regardless of d-c levels at A or B inputs.

description

The '221 and 'LS221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the '121. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With R_{ext} = 2 kΩ and C_{ext} = 0, an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54221, 2 kΩ to 40 kΩ for the SN74221, 2 kΩ to 70 kΩ for the SN54LS221, and 2 kΩ to 100 kΩ for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_{w(out)} = C_{ext}R_{ext}\ ln2 \approx 0.7\ C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is

FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

Also see description and switching characteristics

See explanation of function tables on page 3-8.

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TEXAS INSTRUMENTS
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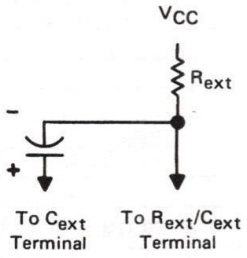
description (continued)

held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

The variance in output pulse width from device to device is typically less than ±0.5% for given external timing components. An example of this distribution for the '221 is shown in Figure 2. Variations in output pulse width versus supply voltage and temperature for the '221 are shown in Figure 3 and 4, respectively.

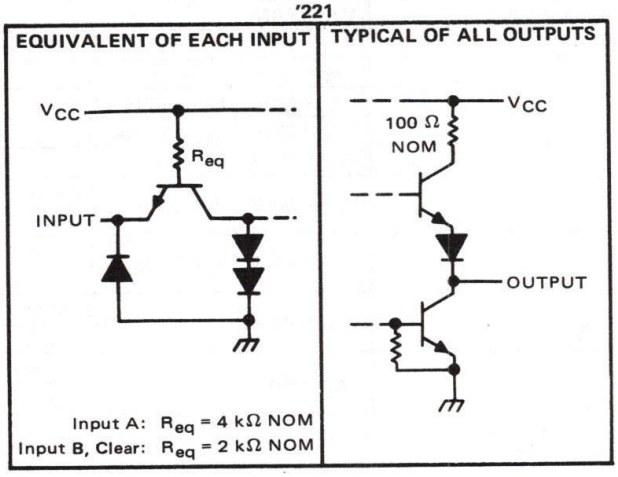
Pin assignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that the '221 or 'LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.



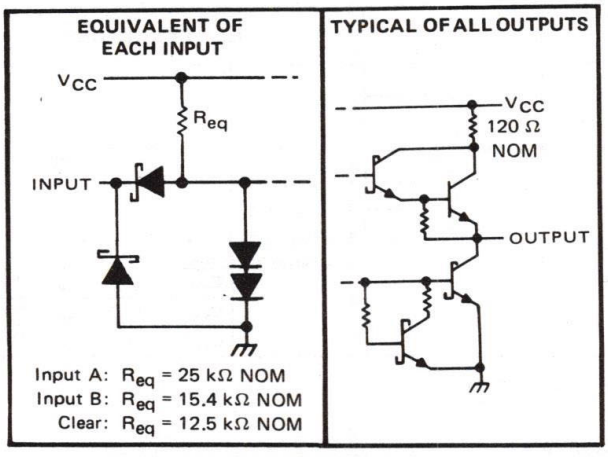
TIMING COMPONENT CONNECTIONS

schematics of inputs and outputs

'221



'LS221



6

recommended operating conditions

		SN54221			SN74221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	50			50			ns
	Clear, $t_{w(clear)}$	20			20			
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4		30	1.4		40	kΩ
External timing capacitance, C_{ext}		0		1000	0		1000	μF
Output duty cycle	R_{ext} = 2 kΩ			67			67	%
	R_{ext} = MAX R_{ext}			90			90	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	Input A			40	μA
			Input B, Clear			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	Input A			−1.6	mA
			Input B, Clear			−3.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54221	−20		−55	mA
			SN74221	−18		−55	
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		26	50	mA
			Triggered		46	80	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1 and Note 2	C_{ext} = 80 pF, R_{ext} = 2 kΩ		45	70	ns
	B	Q				35	55	
t_{PHL}	A	$\overline{Q}$				50	80	ns
	B	$\overline{Q}$				40	65	
t_{PHL}	Clear	Q					27	ns
t_{PLH}	Clear	$\overline{Q}$					40	ns
$t_{w(out)}$	A or B	Q or $\overline{Q}$		C_{ext} = 80 pF, R_{ext} = 2 kΩ	70	110	150	ns
				C_{ext} = 0, R_{ext} = 2 kΩ	20	30	50	
				C_{ext} = 100 pF, R_{ext} = 10 kΩ	650	700	750	
				C_{ext} = 1 μF, R_{ext} = 10 kΩ	6.5	7	7.5	ms

¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
$t_{w(out)}$ ≡ Output pulse width
NOTE 2: Load circuit is shown on page 3-10.

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recommended operating conditions

		SN54LS221			SN74LS221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	40			40			ns
	Clear, $t_{w(clear)}$	40			40			
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4		70	1.4		100	kΩ
External timing capacitance, C_{ext}		0		1000	0		1000	μF
Output duty cycle	R_T = 2 kΩ			50			50	%
	R_T = MAX R_{ext}			90			90	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS221			SN74LS221			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.7	1.0		0.8	1.0		V
V_{T+}	Positive=going threshold voltage at B input	V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.7	0.9		0.8	0.9		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current, Input A	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
	Low-level input current, Input B					−0.8			−0.8	
	Low-level input current, Clear					−0.8			−0.8	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		4.7	11		4.7	11	mA
			Triggered		19	27		19	27	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

6

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_L = 15 pF, R_L = 2 kΩ, See Figure 1 and Note 3	C_{ext} = 80 pF, R_{ext} = 2 kΩ		45	70	ns
	B	Q				35	55	
t_{PHL}	A	$\overline{Q}$				50	80	ns
	B	$\overline{Q}$				40	65	
t_{PHL}	Clear	Q				35	55	ns
t_{PLH}	Clear	$\overline{Q}$				44	65	ns
$t_{w(out)}$	A or B	Q or $\overline{Q}$		C_{ext} = 80 pF, R_{ext} = 2 kΩ	70	120	150	ns
				C_{ext} = 0, R_{ext} = 2 kΩ	20	47	70	
				C_{ext} = 100 pF, R_{ext} = 10 kΩ	600	670	750	
				C_{ext} = 1 μF, R_{ext} = 10 kΩ	6	6.9	7.5	ms

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
$t_{w(out)}$ ≡ Output pulse width

NOTE 3: Load circuit is shown on page 3-11.

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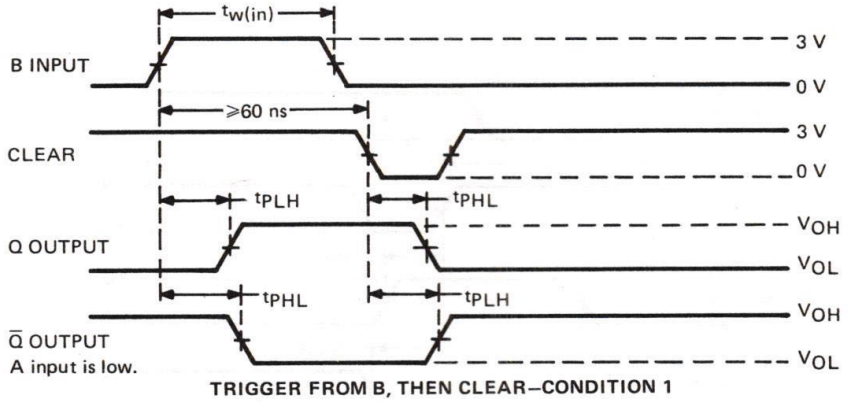
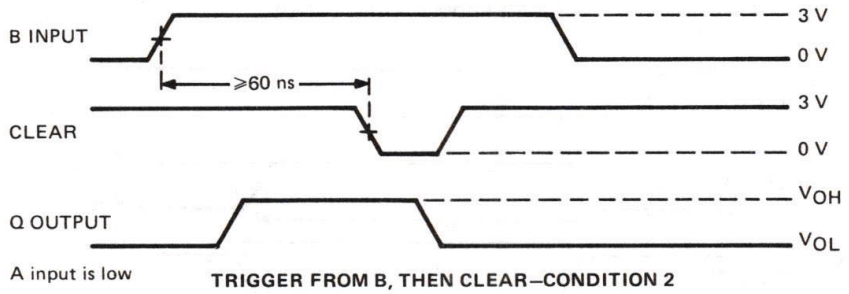
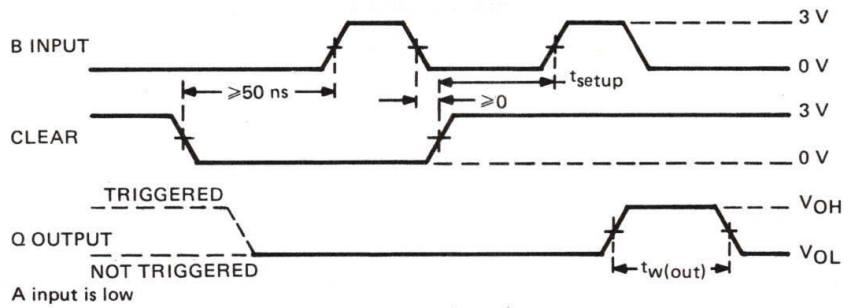
PARAMETER MEASUREMENT INFORMATION



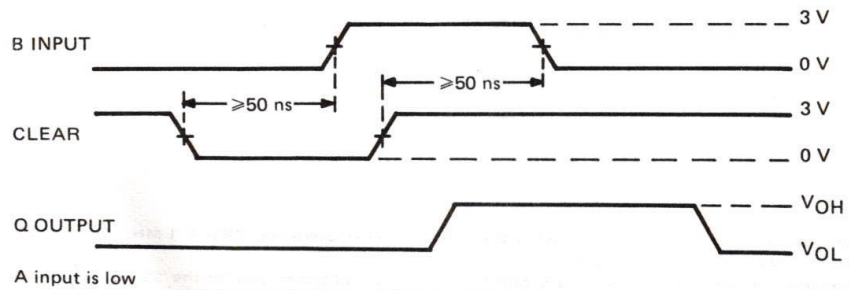
TRIGGER FROM B, THEN CLEAR–CONDITION 1



TRIGGER FROM B, THEN CLEAR–CONDITION 2



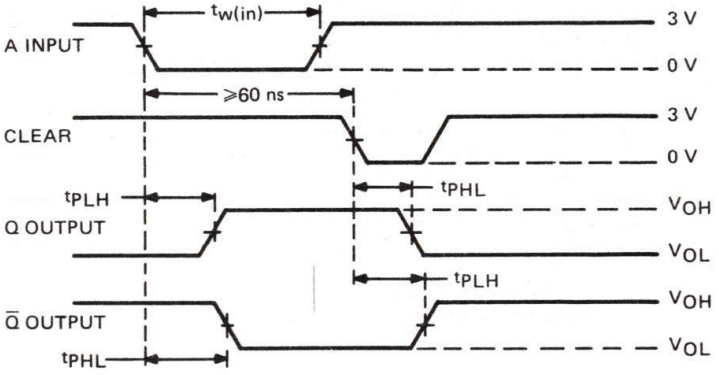
CLEAR OVERRIDING B, THEN TRIGGER FROM B



TRIGGERING FROM POSITIVE TRANSITION OF CLEAR

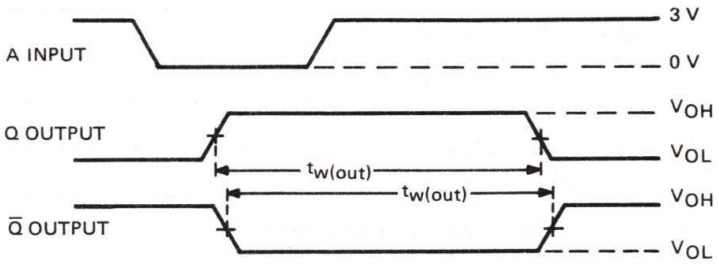
FIGURE 1–SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



B input is high

TRIGGER FROM A, THEN CLEAR



B and clear inputs are high

TRIGGER FROM A

NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, $Z_{out} \approx 50\ \Omega$; for '221, $t_r \leqslant 7$ ns, $t_f \leqslant 7$ ns, for 'LS221, $t_r \leqslant 15$ ns, $t_f \leqslant 6$ ns.
B. All measurements are made between the 1.5 V points of the indicated transitions for the '221 or between the 1.3 V points for the 'LS221.

FIGURE 1–SWITCHING CHARACTERISTICS (CONTINUED)

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TYPICAL CHARACTERISTICS ('221 ONLY)†

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

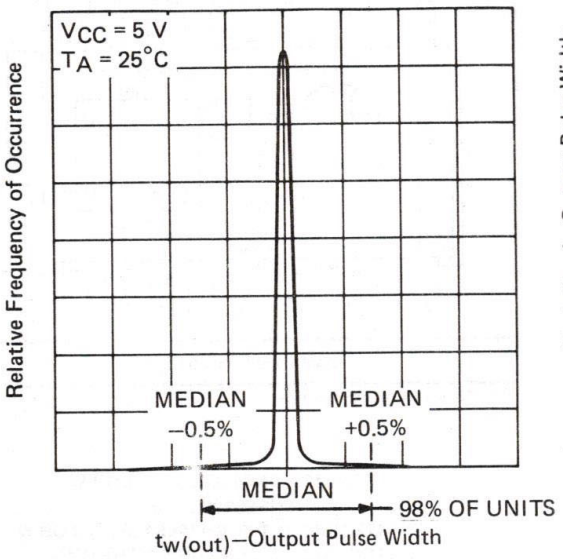


FIGURE 2

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

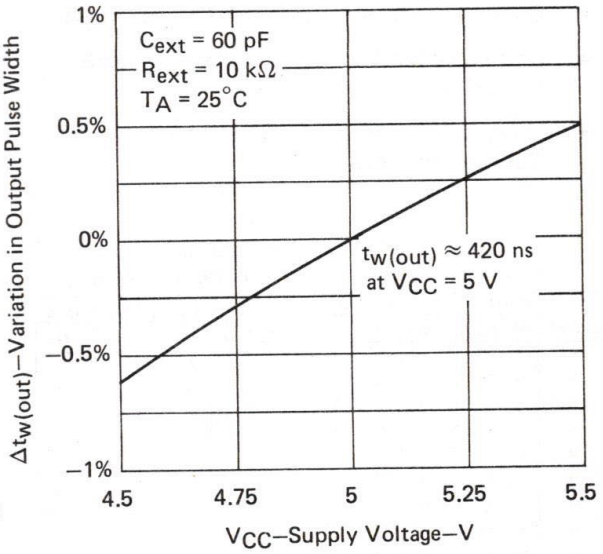


FIGURE 3

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

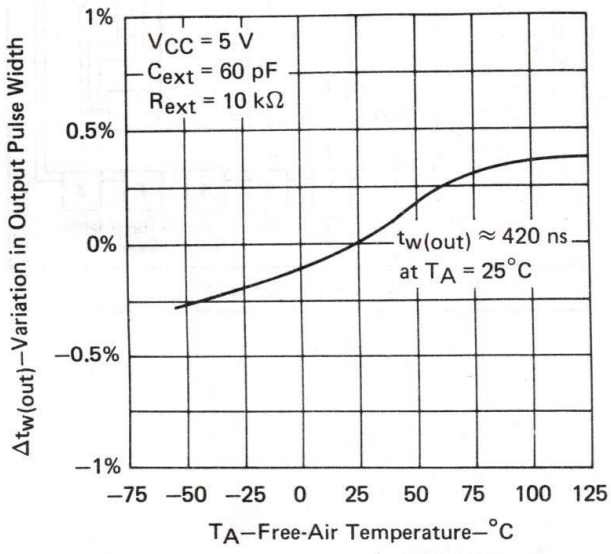


FIGURE 4

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

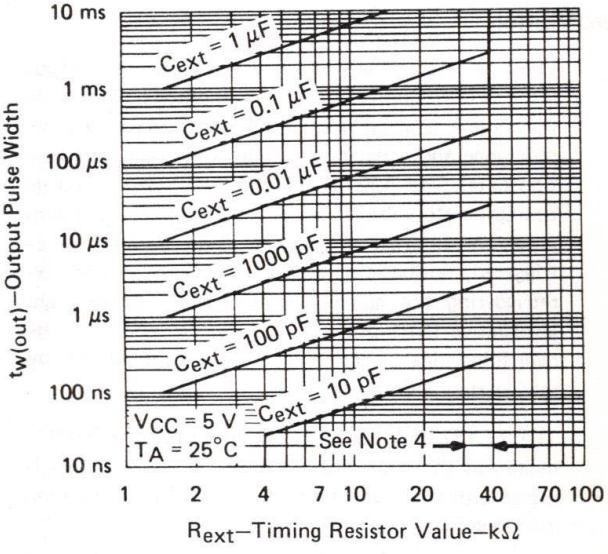


FIGURE 5

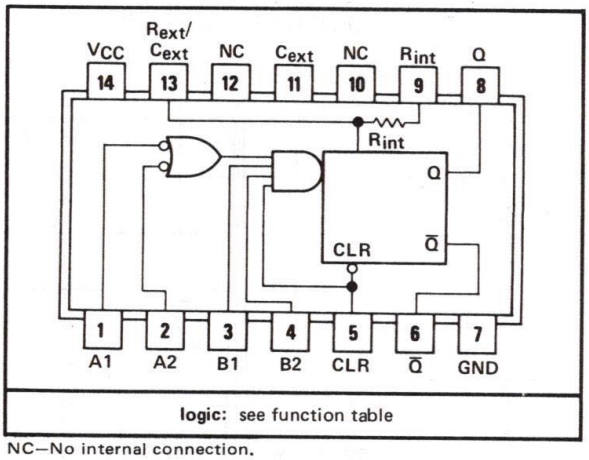
NOTE 4: These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54221.

†Data for temperatures below 0°C and above 70°C, and for supply voltages below 4.75 V and above 5.25 V are applicable for the SN54221 only.

TYPES SN54122, SN54123, SN54L122, SN54L123, SN54LS122, SN54LS123, SN74122, SN74123, SN74L122, SN74L123, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Compensated for V_{CC} and Temperature Variations
- '122, 'L122, 'LS122 Have Internal Timing Resistors

SN54122, SN54LS122 . . . J OR W
SN54L122 . . . J OR T
SN74122, SN74L122, SN74LS122 . . . J OR N
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see function table

NC—No internal connection.

'122, 'L122, 'LS122
FUNCTION TABLE

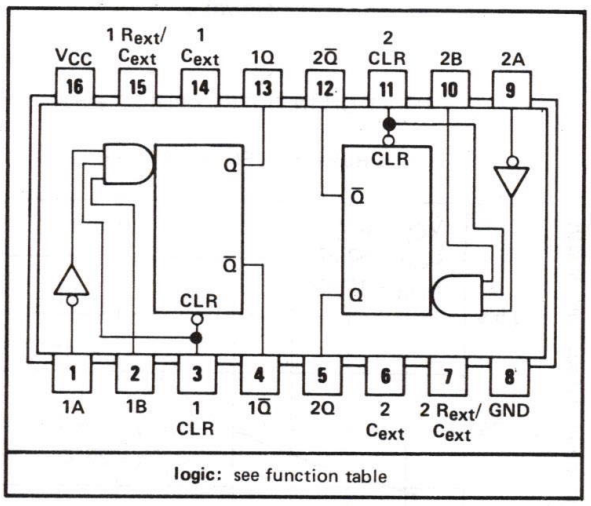
INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	↓	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

'123, 'L123, 'LS123
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

See explanation of function tables on page 3-8.

SN54123, SN54LS123 . . . J OR W
SN54L123 . . . J
SN74123, SN74L123, SN74LS123 . . . J OR N
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see function table

description

These d-c triggered multivibrators feature output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122, 'L122, and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of '122, 'L122 or 'LS122, connect R_{int} to V_{CC}.
3. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

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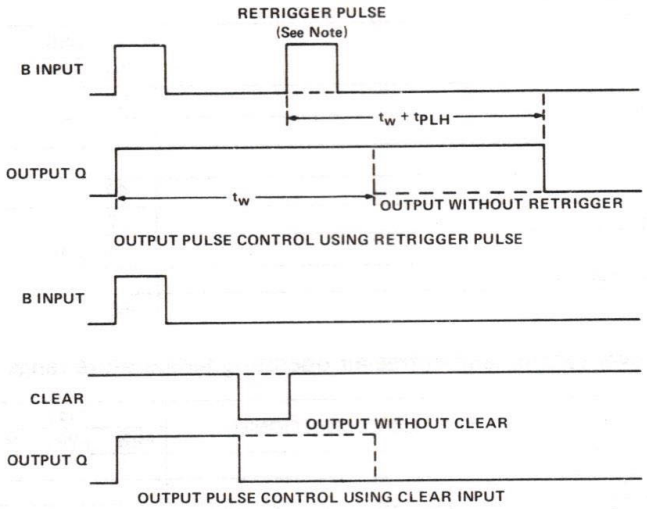
description (continued)



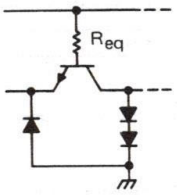
NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

FIGURE 1–TYPICAL INPUT/OUTPUT PULSES

schematics of inputs and outputs

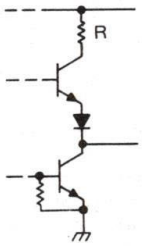
'122, '123, 'L122, 'L123 CIRCUITS

EQUIVALENT OF EACH INPUT



Clear inputs of '122, '123: R_{eq} = 2 kΩ NOM
Other inputs of '122, '123: R_{eq} = 4 kΩ NOM
Clear inputs of 'L122, 'L123: R_{eq} = 4 kΩ NOM
Other inputs of 'L122, 'L123: R_{eq} = 8 kΩ NOM

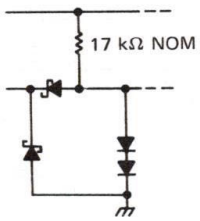
TYPICAL OF ALL OUTPUTS



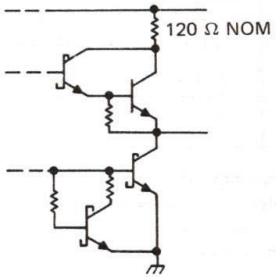
'122, '123: R = 100 Ω NOM
'L122, 'L123: R = 200 Ω NOM

'LS122, 'LS123 CIRCUITS

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



recommended operating conditions

	SN54'			SN74'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		25	5		50	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'122			'123			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −800 μA, See Note 1	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA, See Note 1		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Data inputs	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Clear input				80			80	
I_{IL}	Low-level input current	Data inputs	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Clear input				−3.2			−3.2	
I_{OS}	Short-circuit output current♦		V_{CC} = MAX, See Note 5	−10		−40	−10		−40	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX, See Notes 6 and 7		23	28		46	66	mA

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†For conditions shown as MIN or MAX, use the value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.

6. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 is open.

7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 is open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 8

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'122			'123			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Q	C_{ext} = 0, C_L = 15 pF, R_{ext} = 5 kΩ, R_L = 400 Ω		22	33		22	33	ns
	B				19	28		19	28	
t_{PHL}	A	$\overline{Q}$			30	40		30	40	ns
	B				27	36		27	36	
t_{PHL}	Clear	Q			18	27		18	27	ns
t_{PLH}		$\overline{Q}$			30	40		30	40	
t_{wQ} (min)	A or B	Q			45	65		45	65	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, C_L = 15 pF, R_{ext} = 10 kΩ, R_L = 400 Ω	3.08	3.42	3.76	2.76	3.03	3.37	μs

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{wQ} ≡ width of pulse at output Q

NOTE 8: Load circuit and voltage waveforms are shown on page 3-10.

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recommended operating conditions

	SN54L'			SN74L'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			8			8	mA
Pulse width, t_w	50			50			ns
External timing resistance, R_{ext}	5		25	5		50	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'L122			'L123			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −400 μA, See Note 1	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 8 mA, See Note 1		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Data inputs	V_{CC} = MAX, V_I = 2.4 V			20			20	μA
		Clear input				40			40	
I_{IL}	Low-level input current	Data inputs	V_{CC} = MAX, V_I = 0.4 V			−0.8			−0.8	mA
		Clear input				−1.6			−1.6	
I_{OS}	Short-circuit output current♦		V_{CC} = MAX, See Note 9	−5		−20	−5		−20	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX, See Notes 10 and 11		11	14		23	33	mA

† For conditions shown as MIN or MAX, use the value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦ Not more than one output should be shorted at a time.

NOTES: 9. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
10. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of 'L122 is open.
11. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of 'L122 is open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 8

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'L122			'L123			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Q	C_{ext} = 0, R_{ext} = 5 kΩ, C_L = 15 pF, R_L = 800 Ω		44	66		44	66	ns
	B				38	56		38	56	
t_{PHL}	A	$\overline{Q}$			60	80		60	80	ns
	B				54	72		54	72	
t_{PHL}	Clear	Q			36	54		36	54	ns
t_{PLH}		$\overline{Q}$			60	80		60	80	
t_{wQ} (min)	A or B	Q			90	135		90	135	ns
t_{wQ}	A or B	Q	C_{ext} = 400 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 800 Ω	1.7	1.9	2.1	1.3		2.1	μs

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{wQ} ≡ width of pulse at output Q

NOTE 8: Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX,	See Note 13	'LS122		6	11		6	11	mA
				'LS123		12	20		12	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 12. To measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q, ground R_{ext}/C_{ext}, apply 2 V to B and clear, and pulse A from 2 V to 0 V.
13. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 14

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_{ext} = 0, C_L = 15 pF,	R_{ext} = 5 kΩ, R_L = 2 kΩ		23	33	ns
	B					23	44	
t_{PHL}	A	$\overline{Q}$				32	45	ns
	B					34	56	
t_{PHL}	Clear	Q				20	27	ns
t_{PLH}		$\overline{Q}$				28	45	
t_{wQ} (min)	A or B	Q				116	200	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 2 kΩ	4	4.5	5	μs

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{wQ} ≡ width of pulse at output Q
NOTE 14: Load circuit and voltage waveforms are shown on page 3-11.

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TYPICAL APPLICATION DATA FOR '122, '123, 'L122, 'L123

For pulse widths when $C_{ext} \leq 1000$ pF, See Figures 4 and 5.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = K \cdot R_T \cdot C_{ext}\left(1 + \frac{0.7}{R_T}\right)$$

where

K is 0.32 for '122, 0.28 for '123,
0.37 for 'L122, 0.33 for 'L123

R_T is in kΩ (internal or external timing resistance.

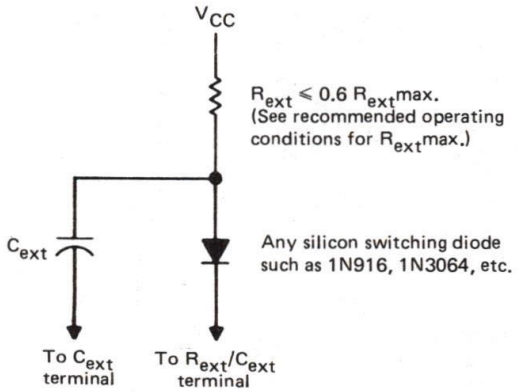
C_{ext} is in pF

t_w is in nanoseconds

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure 2 be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

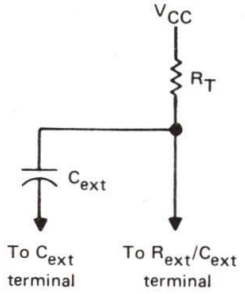
$$t_w = K_D \cdot R_T \cdot C_{ext}\left(1 + \frac{0.7}{R_T}\right)$$

K_D is 0.28 for '122, 0.25 for '123,
0.33 for 'L122, 0.29 for 'L123



TIMING COMPONENT CONNECTIONS WHEN $C_{ext} > 1000$ pF AND CLEAR IS USED
FIGURE 2

Applications requiring more precise pulse widths (up to 28 seconds) and not requiring the clear feature can best be satisfied with the '121 or 'L121.



TIMING COMPONENT CONNECTIONS
FIGURE 3

'122, '123
TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

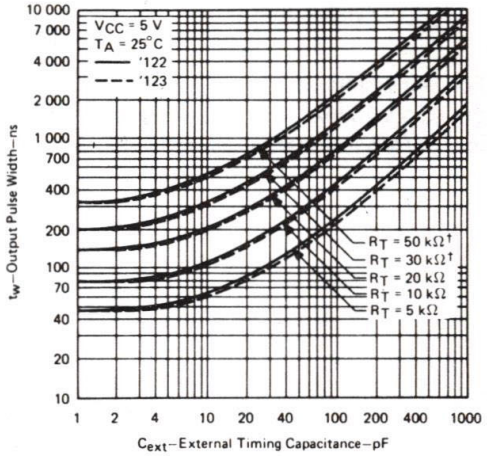


FIGURE 4

'L122
TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

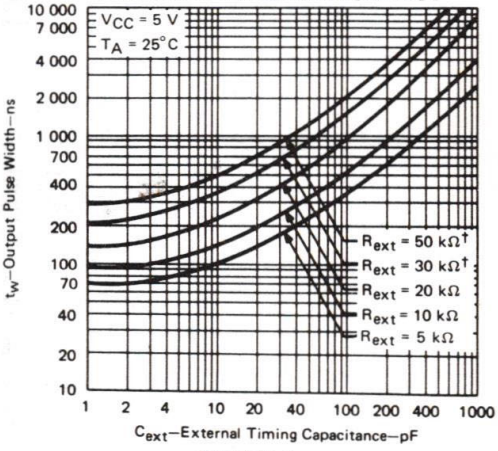


FIGURE 5

†These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54' and SN54L' circuits.

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TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq 1000$ pF, see Figure 7.

When $C_{ext} > 1000$ pF, the output pulse width is defined as:

$$t_w = 0.45 \cdot R_T \cdot C_{ext}$$

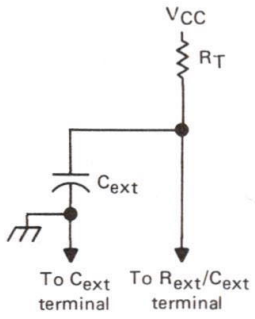
where

R_T is in kΩ (internal or external timing resistance.)

C_{ext} is in pF

t_w is in nanoseconds

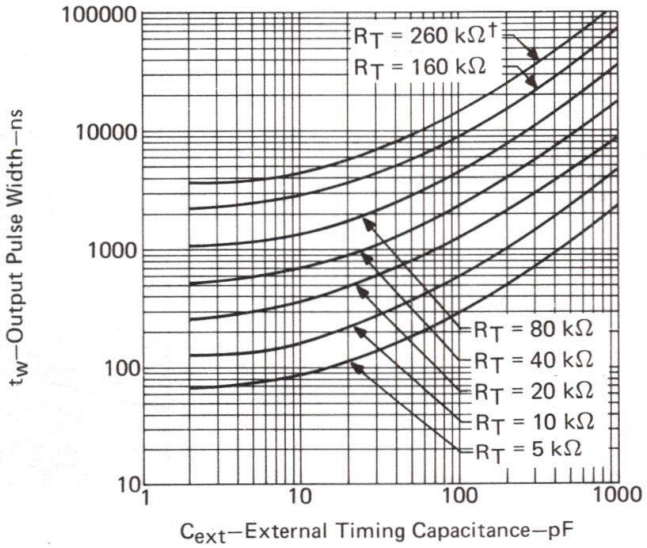
For best results, system ground should be applied to the C_{ext} terminal. The switching diode is not needed for electrolytic capacitance applications.



TIMING COMPONENT CONNECTIONS

FIGURE 6

'LS122, 'LS123
TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE



† This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 7

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TYPES SN54LS240,SN54LS241,SN54LS244,SN54S240,SN54S241, SN74LS240,SN74LS241,SN74LS244,SN74S240,SN74S241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

	Typical I_{OL} (Sink Current)	Typical I_{OH} (Source Current)	Typical Propagation Delay Times		Typical Enable/ Disable Times	Typical Power Dissipation (Enabled)	
			Inverting	Noninverting		Inverting	Noninverting
SN54LS'	12 mA	−12 mA	10,5 ns	12 ns	18 ns	130 mW	135 mW
SN74LS'	24 mA	−15 mA	10,5 ns	12 ns	18 ns	130 mW	135 mW
SN54S'	48 mA	−12 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW
SN74S'	64 mA	−15 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW

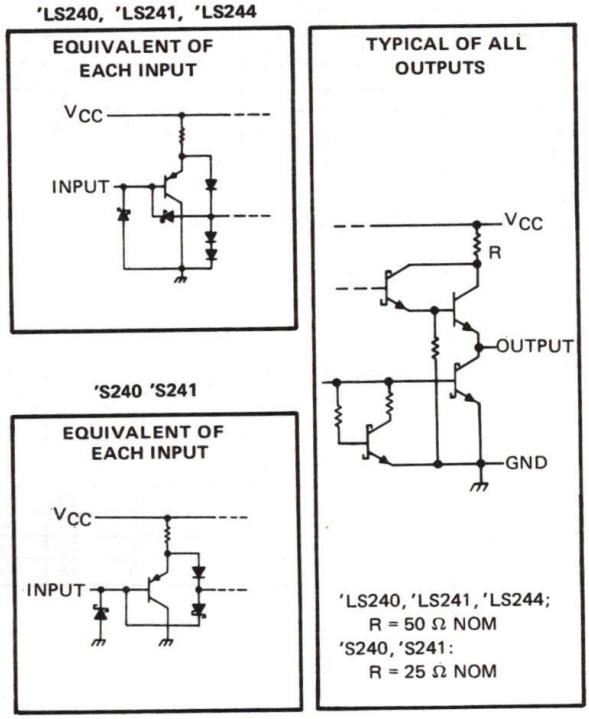
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce D-C Loading**
- **Hysteresis at Inputs Improves Noise Margins**

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

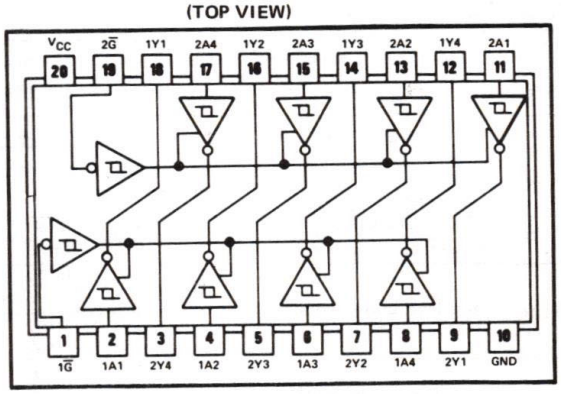
schematics of inputs and outputs

'LS240, 'LS241, 'LS244

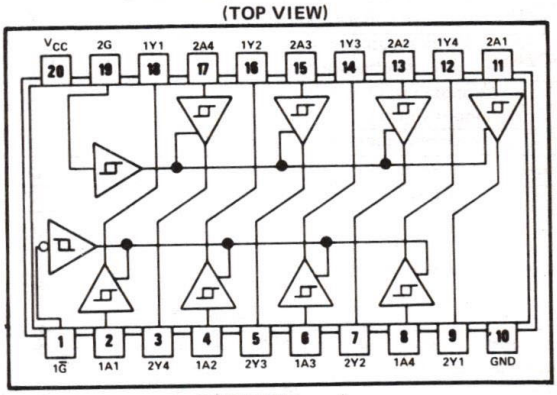


'S240 'S241

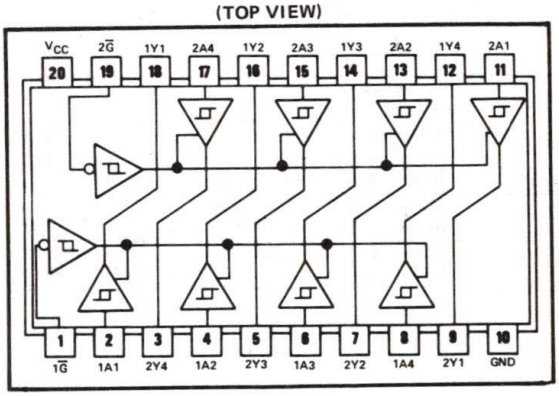
SN54LS240, SN54S240 . . . J
SN74LS240, SN74S240 . . . J OR N
(TOP VIEW)



SN54LS241, SN54S241 . . . J
SN74LS241, SN74S241 . . . J OR N
(TOP VIEW)



SN54LS244 . . . J
SN74LS244 . . . J OR N
(TOP VIEW)



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TEXAS INSTRUMENTS
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recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA			0.4			0.4	V
			I_{OL} = 24 mA						0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current, any input	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_{IL} = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open	All		17	27		17	27	mA
		Outputs low		'LS240		26	44		26	44	
				'LS241, 'LS244		27	46		27	46	
		All outputs disabled		'LS240		29	50		29	50	
				'LS241, 'LS244		32	54		32	54	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, See Note 2	R_L = 667 Ω,		9	14		12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	18		12	18	ns
t_{PZL}	Output enable time to low level				20	30		20	30	ns
t_{PZH}	Output enable time to high level				15	23		15	23	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 2	R_L = 667 Ω,		15	25		15	25	ns
t_{PHZ}	Output disable time from high level				10	18		10	18	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

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recommended operating conditions

PARAMETER	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			48			64	mA
External resistance between any input or V_{CC} and ground			40			40	kΩ
Operating free-air temperature, T_A (see Note 3)	−55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
3. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'S240			'S241			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	SN74S'	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	2.7			2.7			V
		SN54S' and SN74S'	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
		SN54S' and SN74S'	V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.55			0.55	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.5 V			−50			−50	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current, any input		V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current	Any A	V_{CC} = MAX,	V_I = 0.5 V			−400			−400	μA
		Any G					−2			−2	mA
I_{OS}	Short-circuit output current♦		V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open	SN54S'		80	123		95	147	mA
				SN74S'		80	135		95	160	
		Outputs low		SN54S'		100	145		120	170	
				SN74S'		100	150		120	180	
		Outputs disabled		SN54S'		100	145		120	170	
				SN74S'		100	150		120	180	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'S240			'S241			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Note 4	R_L = 90 Ω,		4.5	7		6	9	ns
t_{PHL}	Propagation delay time, high-to-low-level output				4.5	7		6	9	ns
t_{PZL}	Output enable time to low level				10	15		10	15	ns
t_{PZH}	Output enable time to high level				6.5	10		8	12	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 4	R_L = 90 Ω,		10	15		10	15	ns
t_{PHZ}	Output disable time from high level				6	9		6	9	ns

NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

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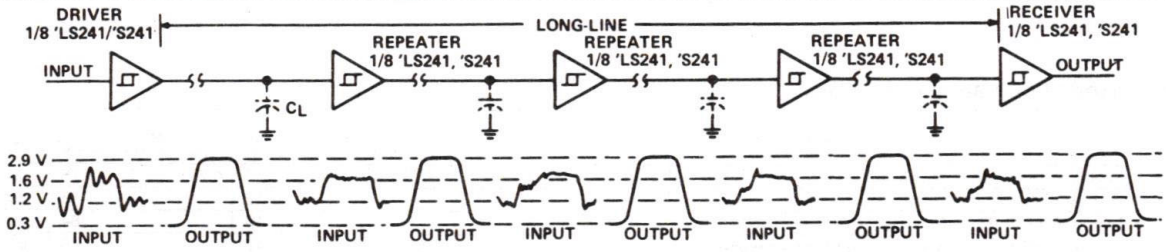
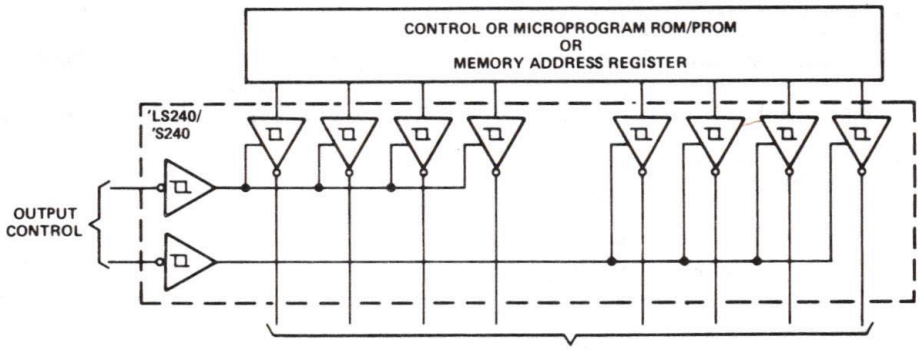
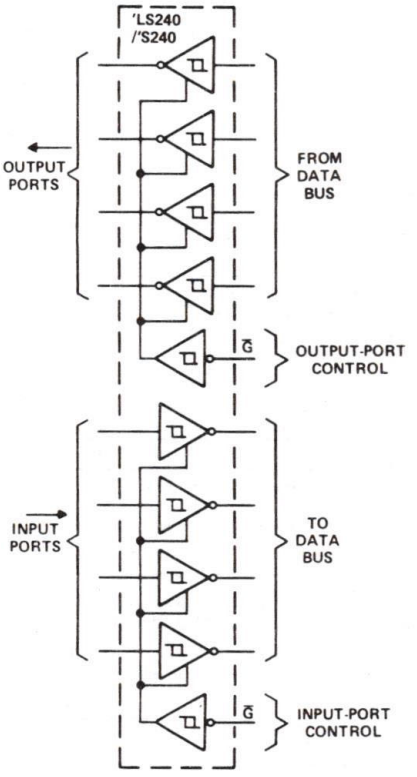


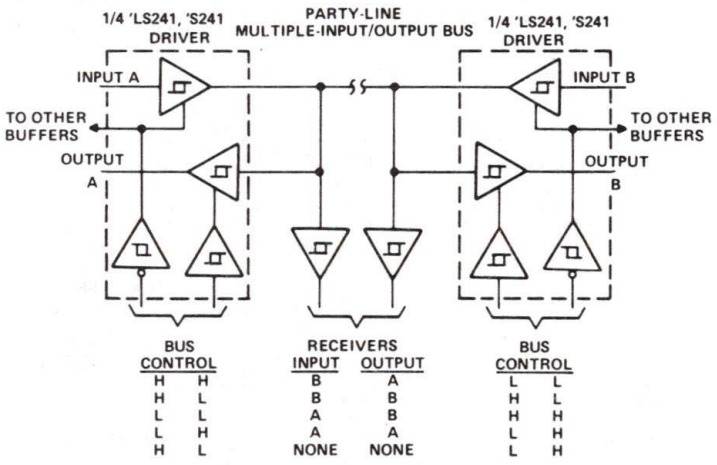
'LS241, 'S241 USED AS REPEATER/LEVEL RESTORER



'LS241, 'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

External resistance between any input of the 'S240 or 'S241 and ground or V_{CC} must not exceed 40 kΩ.

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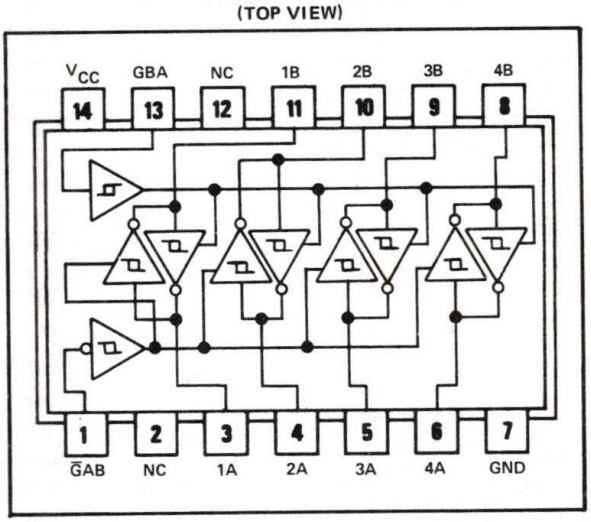
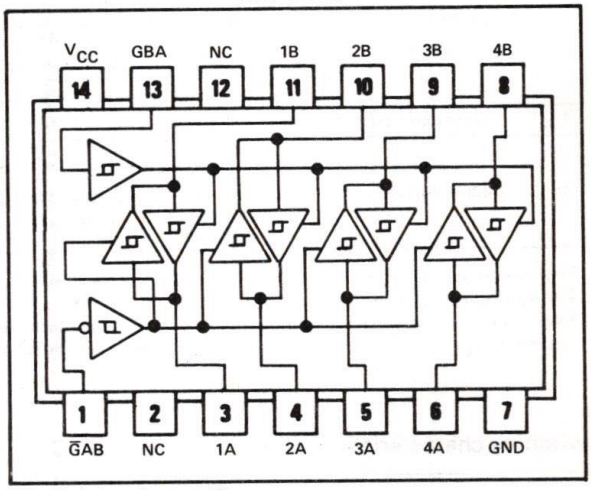
TYPES SN54LS242, SN54LS243, SN74LS242, SN74LS243
QUADRUPLE BUS TRANSCEIVERS

- **Two-Way Asynchronous Communication Between Data Buses**
- **P-N-P Inputs Reduce D-C Loading**
- **Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin**

SN54LS242 . . . J OR W
SN74LS242 . . . J OR N
(TOP VIEW)



SN54LS243 . . . J OR W
SN74LS243 . . . J OR N
(TOP VIEW)



NC—No internal connection

description

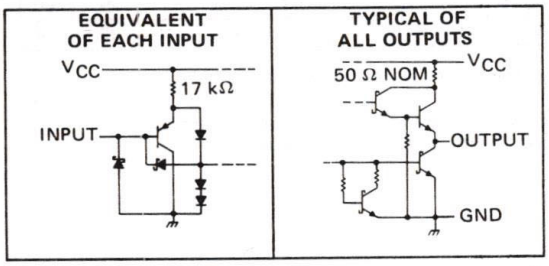
These four-data-line transceivers are designed for asynchronous two-way communications between data buses. The SN74LS' can be used to drive terminated lines down to 133 ohms.

FUNCTION TABLE (EACH TRANSCEIVER)

CONTROL INPUTS		'LS242 DATA PORT STATUS		'LS243 DATA PORT STATUS	
$\overline{G}AB$	GBA	A	B	A	B
H	H	$\overline{O}$	I	O	I
L	H	*	*	*	*
H	L	ISOLATED		ISOLATED	
L	L	I	$\overline{O}$	I	O

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.
I = Input, O = Output, $\overline{O}$ = Inverting Output.

schematics of inputs and outputs



recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.1		2.4	3.1		V
			V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max	V_O = 2.7 V			40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−200			−200	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		$\overline{G}$AB or GBA		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current, any input		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	A inputs	V_{CC} = MAX,	V_I = 0.4 V, $\overline{G}$AB and GBA at 0 V			−0.2			−0.2	mA
		B inputs	V_{CC} = MAX,	V_I = 0.4 V, $\overline{G}$AB and GBA at 4.5 V			−0.2			−0.2	
		$\overline{G}$AB or GBA	V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	
I_{OS}	Short-circuit output current◆		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open, See Note 2	'LS242, 'LS243		22	38		22	38	mA
		Outputs low		'LS242, 'LS243		29	50		29	50	
		All outputs disabled		'LS242		29	50		29	50	
				'LS243		32	54		32	54	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
◆Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with transceivers enabled in one direction only, or with all transceivers disabled.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'LS242 MIN	'LS242 TYP	'LS242 MAX	'LS243 MIN	'LS243 TYP	'LS243 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, See Note 3	R_L = 667 Ω,		9	14		12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	18		12	18	ns
t_{PZL}	Output enable time to low level				20	30		20	30	ns
t_{PZH}	Output enable time to high level				15	23		15	23	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 3	R_L = 667 Ω,		15	25		15	25	ns
t_{PHZ}	Output disable time from high level				10	18		10	18	ns

NOTE 3: Load circuit and waveforms are shown on page 3-11.

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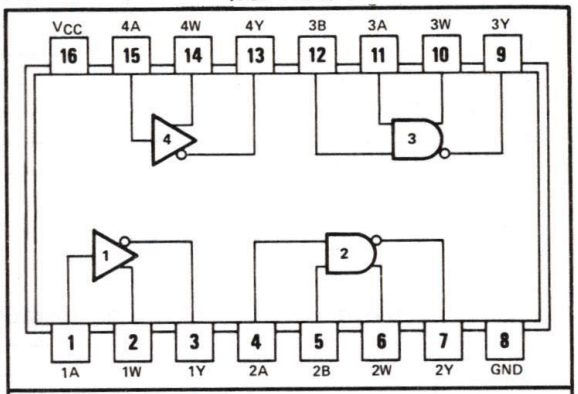
FOR SYMMETRICAL GENERATION OF COMPLEMENTARY TTL SIGNALS

- **Switching Time Skew of the Complementary Outputs Is Typically 0.5 ns . . . Guaranteed to be No More than 3 ns at Rated Loading**
- **Full Fan-Out to 20 High-Level and 10 Low-Level 54/74 Loads**
- **Active Pull-Down Provides Square Transfer Characteristic**

SN54265 . . . J OR W PACKAGE
SN74265 . . . J OR N PACKAGE
(TOP VIEW)



positive logic:

ELEMENTS 1 AND 4	ELEMENTS 2 AND 3
$Y = \overline{A}$	$Y = \overline{AB}$
$W = A$	$W = AB$

description

The SN54265 and SN74265 circuits feature complementary outputs from each logic element, which have virtually symmetrical switching time delays from the triggering input. They are designed specifically for use in applications such as:

- Symmetrical clock/$\overline{\text{clock}}$ generators
- Complementary input circuit for decoders and code converters
- Switch debouncing
- Differential line driver

Examples of these four functions are illustrated in the typical application data.

The SN54265 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74265 is characterized for operation from 0°C to 70°C.

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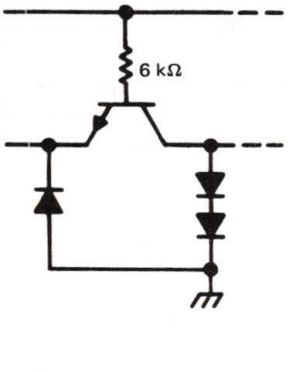
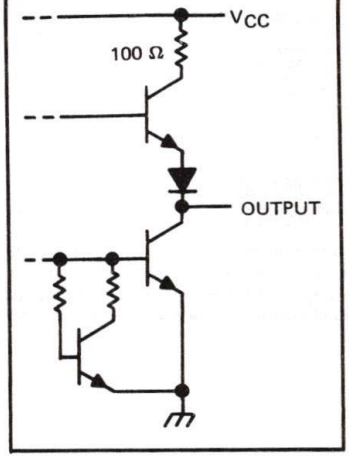
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



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recommended operating conditions

	SN54265			SN74265			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = −800 μA	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,	SN54265	−20		−57	mA
			SN74265	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		25	34	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(W)}$	A or B (as applicable)	W	R_L = 400 Ω, C_L = 15 pF, See Note 4		11.6	18	ns
$t_{PHL(Y)}$		Y			11.3	18	
$t_{PHL(W)}$	A or B (as applicable)	W			9.8	18	ns
$t_{PLH(Y)}$		Y			10.2	18	
$t_{PLH(W)}-t_{PHL(Y)}$	A or B (as applicable)	W with respect to Y			+0.3	±3	ns
$t_{PHL(W)}-t_{PLH(Y)}$					−0.4	±3	

t_{PLH} ≡ Propagation delay time, low-to-high-level output.
t_{PHL} ≡ Propagation delay time, high-to-low-level output.
$t_{PXX(W)}-t_{PXX(Y)}$ ≡ Difference in indicated propagation delay times at the W and Y outputs, respectively.
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

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TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME DIFFERENCE
vs
FREE-AIR TEMPERATURE

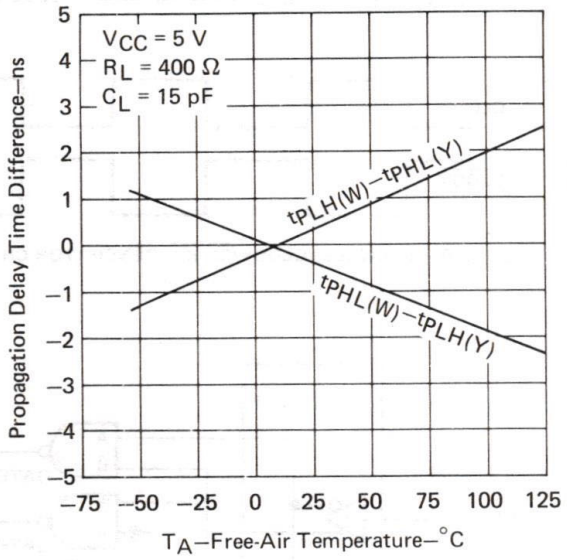

FIGURE 1

PROPAGATION DELAY TIME DIFFERENCE
vs
SUPPLY VOLTAGE

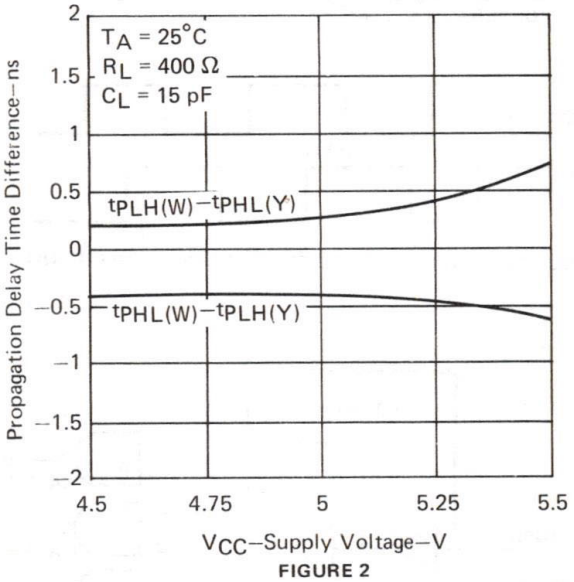

FIGURE 2

PROPAGATION DELAY TIME DIFFERENCE vs LOAD CAPACITANCE

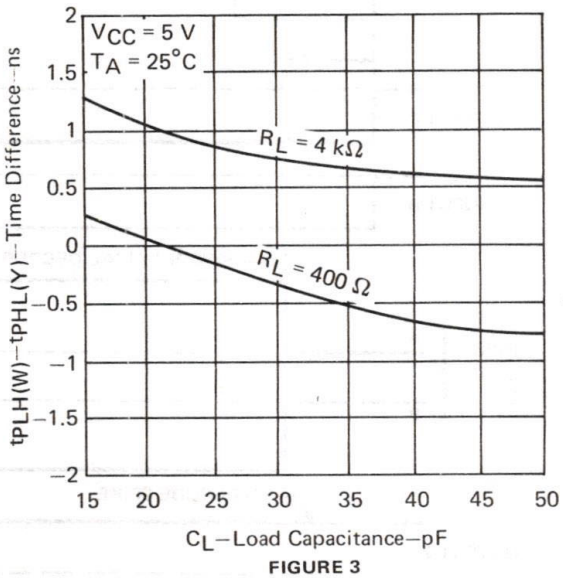

FIGURE 3

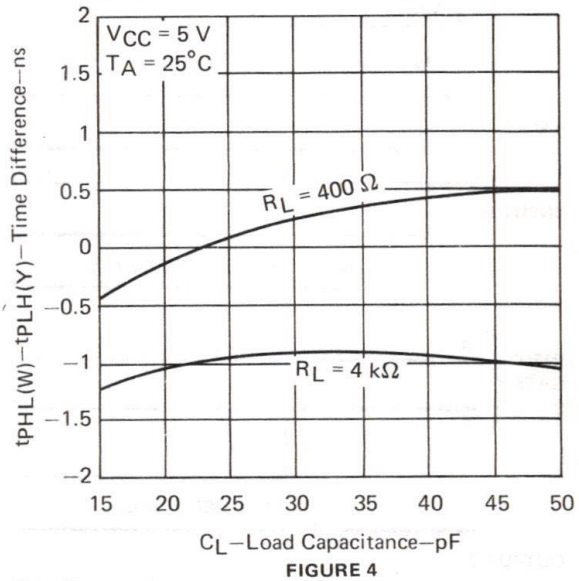

FIGURE 4

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54265 only.

TYPICAL APPLICATION DATA

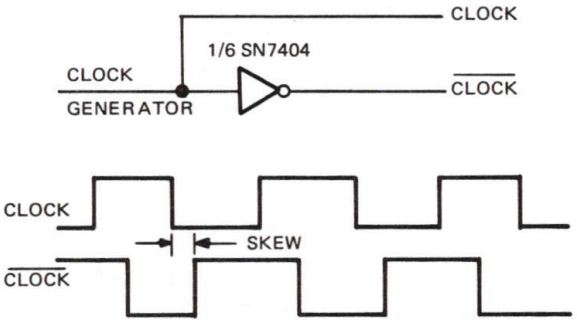

FIGURE A – TYPICAL CLOCK/$\overline{\text{CLOCK}}$ GENERATOR CIRCUIT

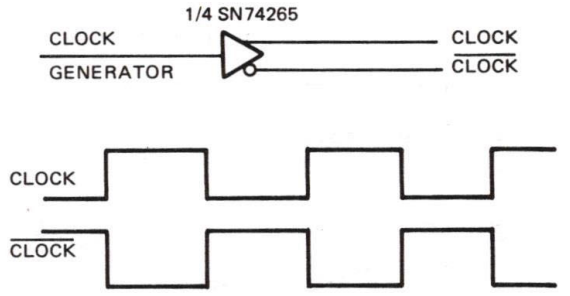

FIGURE B – SKEWLESS CLOCK/$\overline{\text{CLOCK}}$ GENERATOR CIRCUIT

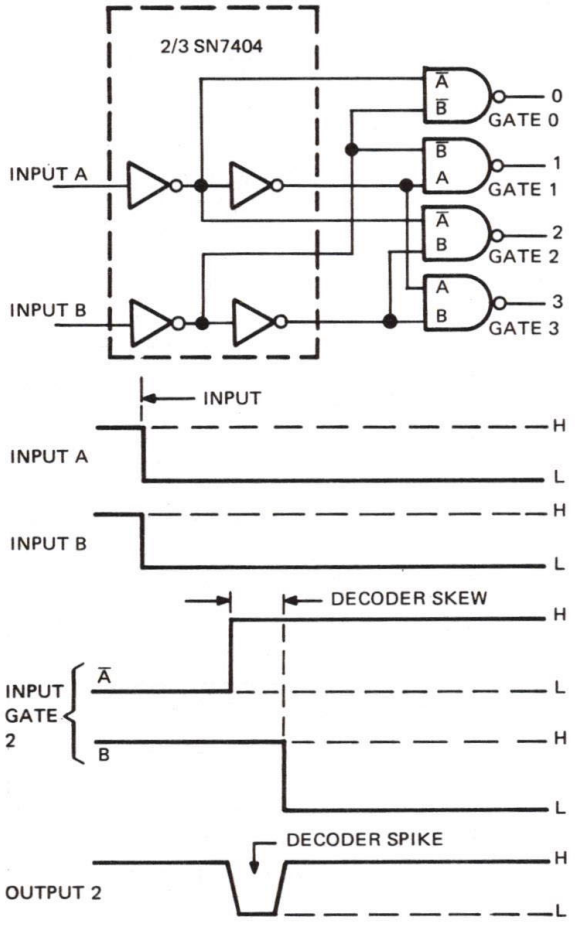

FIGURE C – TYPICAL DECODER/CODE CONVERTER

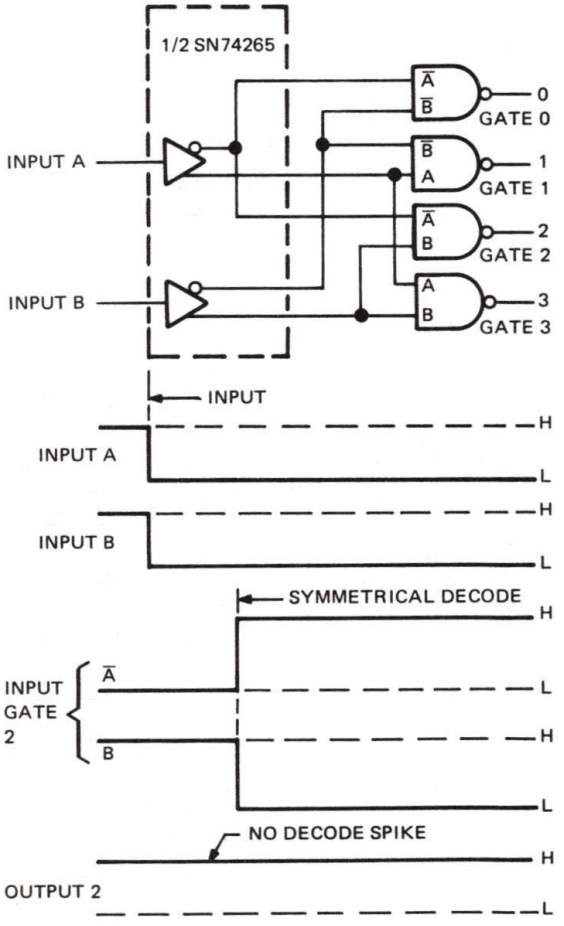

FIGURE D – SYMMETRICAL DECODER/CODE CONVERTER

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TYPICAL APPLICATION DATA

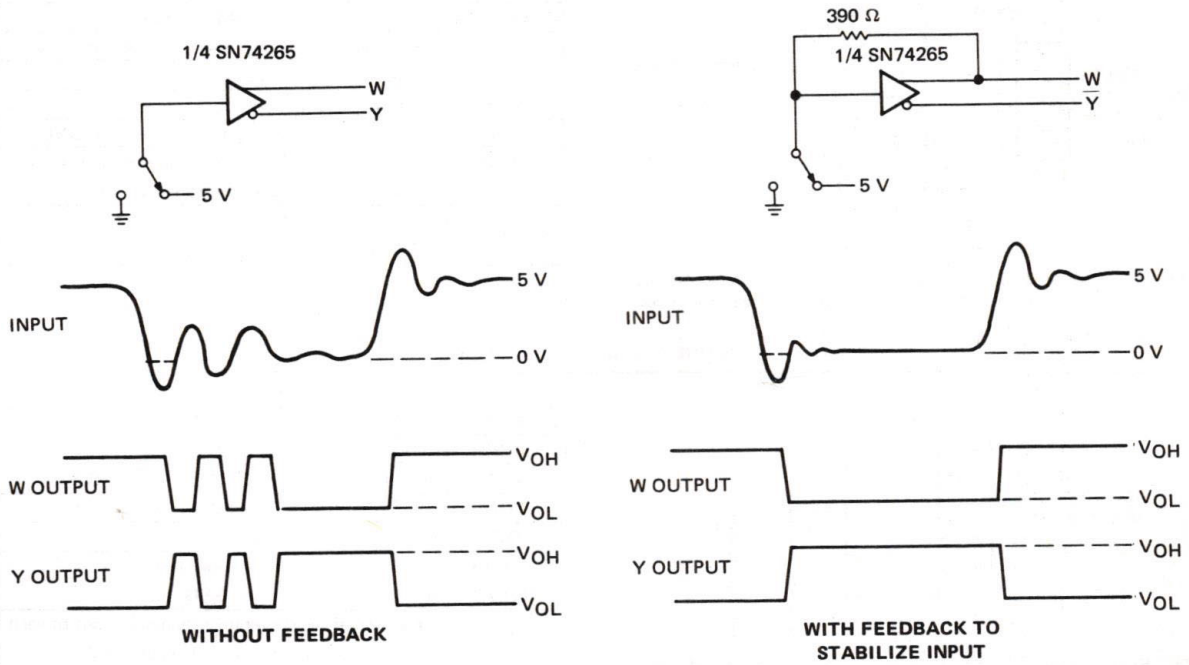
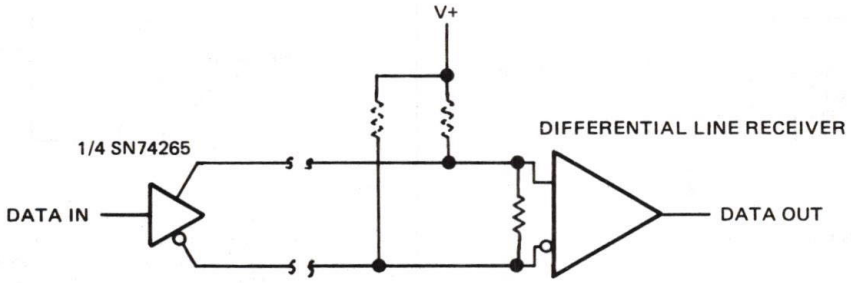


FIGURE E – SWITCH DEBOUNCER



Noise immunity typically 3 V
for either high level or low level data

FIGURE F – DIFFERENTIAL LINE DRIVER

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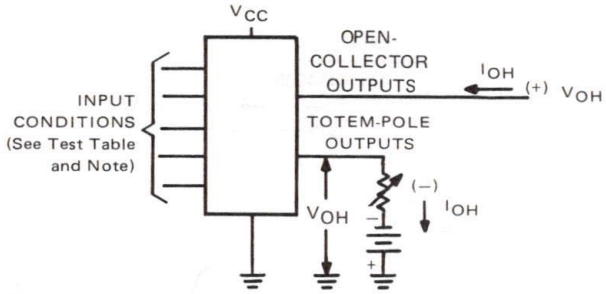
PARAMETER MEASUREMENT INFORMATION

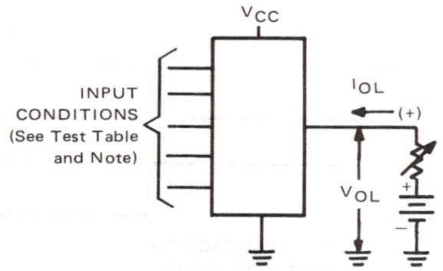


NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	Input under test at V_{IL} max, all others at 4.5 V
AND	All inputs at V_{IH} min
NOR	All inputs at V_{IL} max
OR	Input under test at V_{IH} min, all others at GND
AND-OR-INVERT	Inputs under test (a set including one input of each AND gate) at V_{IL} max, all others at 4.5 V
AND-OR	All inputs of AND gate under test at V_{IH} min, all others at GND

FIGURE 1–V_{IH}, V_{IL}, V_{OH}, I_{OH}



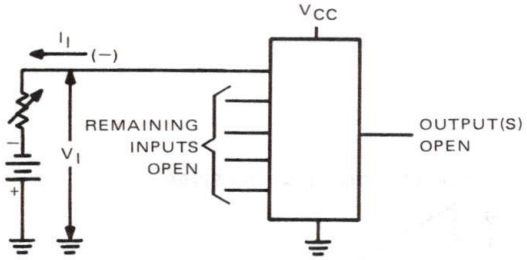
NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	All inputs at V_{IH} min
AND	Input under test at V_{IL} max, all others at 4.5 V
NOR	Input under test at V_{IH} min, others at GND
OR	All inputs at V_{IL} max
AND-OR-INVERT	All inputs of AND gate under test at V_{IH} min, all others at GND
AND-OR	Inputs under test (a set including one input of each AND gate) at V_{IH} min, all others at 4.5 V

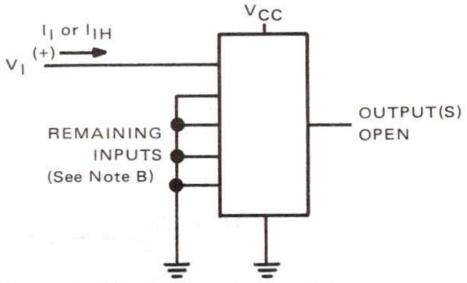
FIGURE 2–V_{IH}, V_{IL}, V_{OL}

6



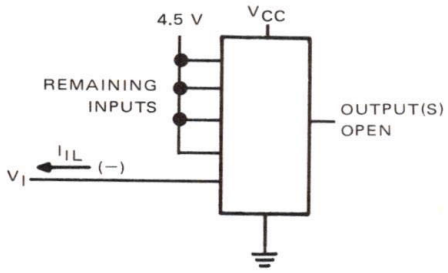
NOTE: Each input is tested separately.

FIGURE 3–V_I



NOTES: A. Each input is tested separately.
B. When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with inputs of AND gates not under test open when testing I_I and grounded when testing I_{IH}.

FIGURE 4–I_I, I_{IH}



NOTES: A. Each input is tested separately.
B. When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with inputs of AND gates not under test open.

FIGURE 5–I_{IL}

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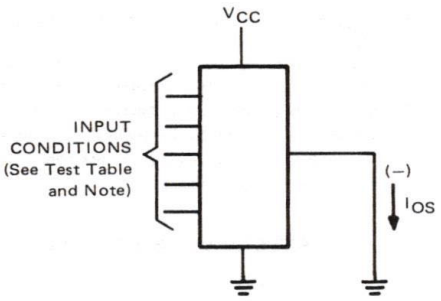
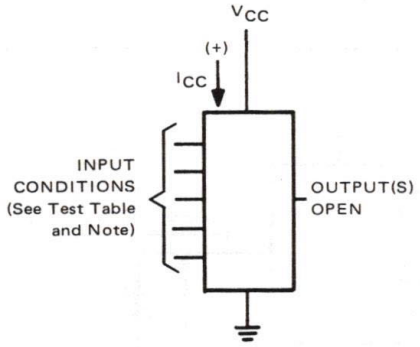


TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	All inputs at GND
AND	All inputs at 4.5 V
NOR	All inputs at GND
OR	All inputs at 4.5 V
AND-OR-INVERT	All inputs at GND
AND-OR	All inputs at 4.5 V

NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

FIGURE 6–I_{OS}



TEST TABLE

FUNCTION	INPUT CONDITIONS FOR I_{CCH}	INPUT CONDITIONS FOR I_{CCL}
NAND	All inputs at GND	All inputs at 4.5 V
AND	All inputs at 4.5 V	All inputs at GND
NOR	All inputs at GND	One input at 4.5 V, all others at GND
OR	One input at 4.5 V, all others at GND	All inputs at GND
AND-OR-INVERT	All inputs at GND	All inputs of one AND gate at 4.5 V, all others at GND
AND-OR	All inputs of one AND gate at 4.5 V, all others at GND	All inputs at GND

NOTE: I_{CC} is measured simultaneously for all functions in a package. The average-per-gate values are calculated from the appropriate one of the following equations:

$$I_{CC},\ I_{CCH},\ \text{or}\ I_{CCL}\ \text{(average per gate or flip-flop)} = \frac{\text{total } I_{CC},\ I_{CCH},\ \text{or } I_{CCL}}{\text{(number of gates or flip-flops in package)}}$$

$$I_{CC}\ \text{(average per gate, 50\% duty cycle)} = \frac{I_{CCH} + I_{CCL}}{2\ \text{(number of gates in package)}}$$

FIGURE 7–I_{CC}

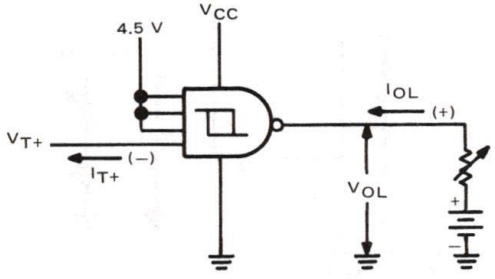


FIGURE 8–V_{T+}, I_{T+}, V_{OL} (FOR NAND SCHMITT TRIGGERS)

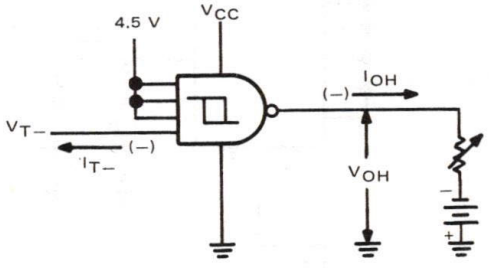
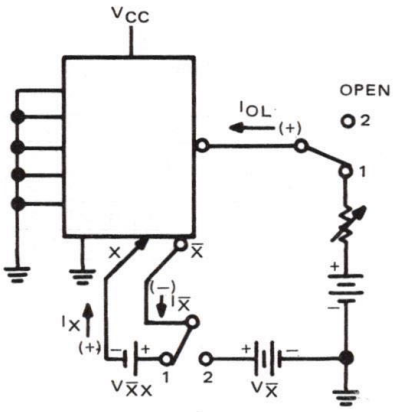


FIGURE 9–V_{T-}, I_{T-}, V_{OH} (FOR NAND SCHMITT TRIGGERS)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Switches are in position 1 for SN54'/SN74', position 2 for SN54H'/SN74H'.

B. The $I_{\overline{X}}$ limit for SN54' and SN74' circuits may be verified by an alternate equivalent procedure. The $V_{\overline{X}X}$ source is replaced by a resistor (see table below) in parallel with a voltmeter between the X and $\overline{X}$ pins. If the measured voltage, $V_{\overline{X}X}$, is less than 0.4, the specified limit for $I_{\overline{X}}$ is met.

RESISTANCE VALUE TABLE

SN5423	114 Ω
SN5450, SN5453	138 Ω
SN7423	105 Ω
SN7450, SN7453	130 Ω

FIGURE 10–$I_{\overline{X}}$ (FOR EXPANDABLE GATES)

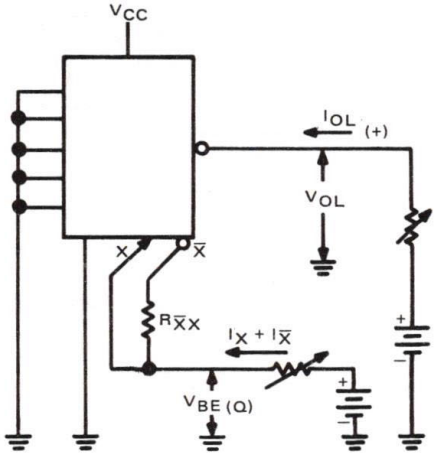


FIGURE 11–$V_{BE(Q)}$ (FOR EXPANDABLE GATES)

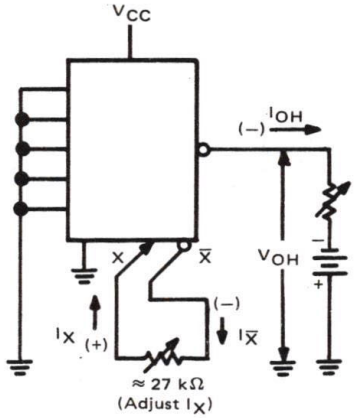


FIGURE 12–V_{OH} (FOR EXPANDABLE GATES)

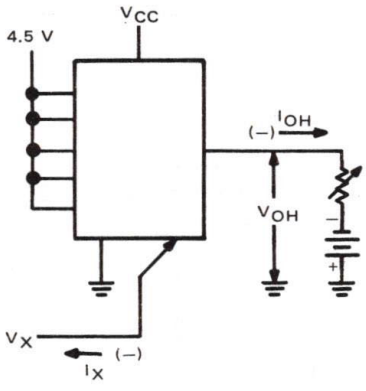


FIGURE 13–V_{OH} (FOR EXPANDABLE GATES)

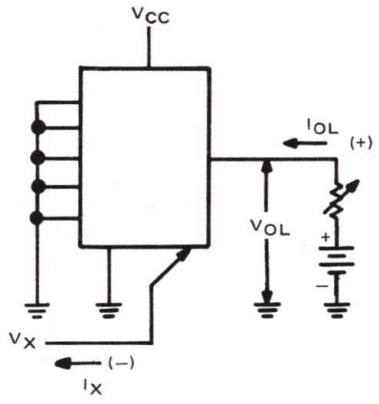


FIGURE 14–V_{OL} (FOR EXPANDABLE GATES)

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PARAMETER MEASUREMENT INFORMATION

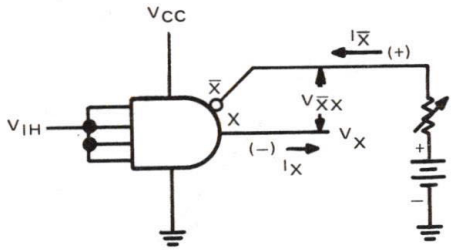


FIGURE 15—ON-STATE CHARACTERISTICS FOR EXPANDERS

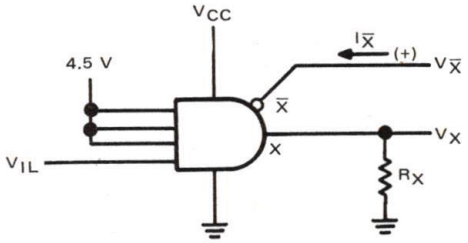


FIGURE 16—OFF-STATE CHARACTERISTICS FOR EXPANDERS

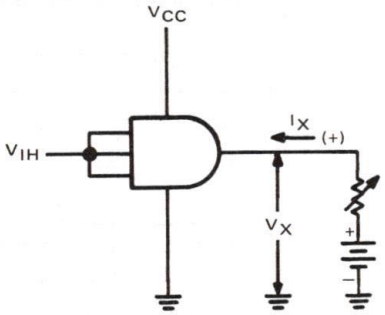


FIGURE 17—ON-STATE CHARACTERISTICS FOR EXPANDERS

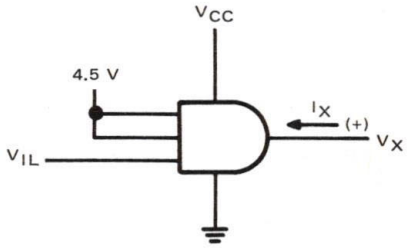
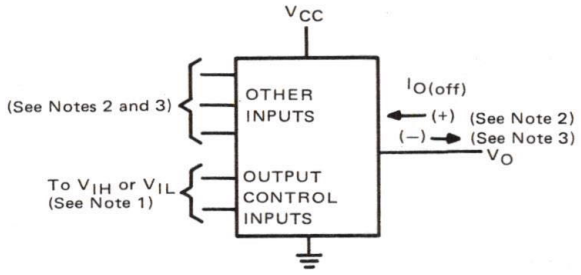


FIGURE 18—OFF-STATE CHARACTERISTICS FOR EXPANDERS



NOTES: 1. Input conditions are maintained which will ensure that the three-state output(s) is (are) disabled to the high-impedance state. See function table or logic for the particular device.
2. When testing for current into the output with a high-level output voltage, input conditions are applied that would cause the output to be low if it were enabled.
3. When testing for current out of the output with a low-level output voltage, input conditions are applied that would cause the output to be high if it were enabled.

FIGURE 19—$I_{O(off)}$ (THREE-STATE OUTPUTS)

TYPICAL CHARACTERISTICS†§

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

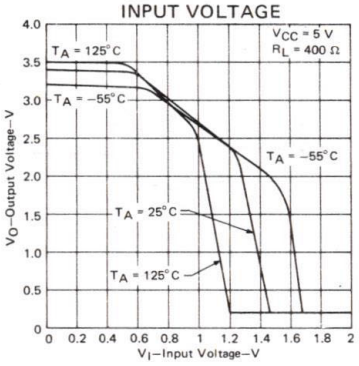


FIGURE A1

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

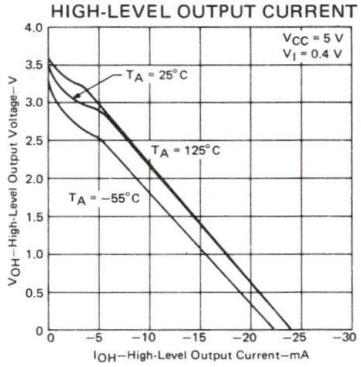


FIGURE A2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

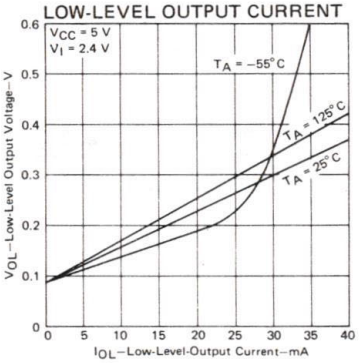


FIGURE A3

AVERAGE PROPAGATION DELAY TIME,
vs
FREE-AIR TEMPERATURE

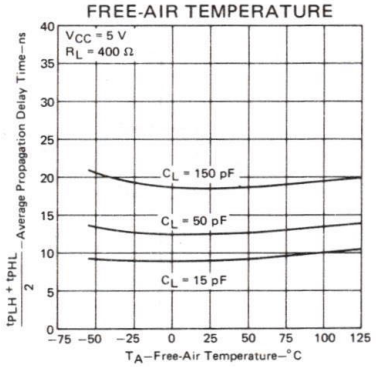


FIGURE A4

PROPAGATION DELAY TIME,
LOW-TO-HIGH LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

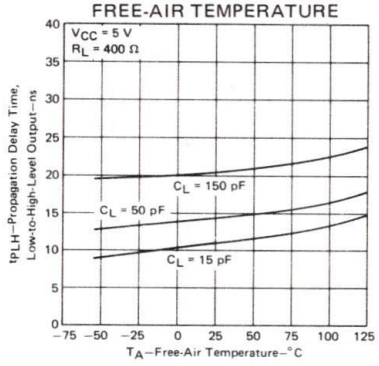


FIGURE A5

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

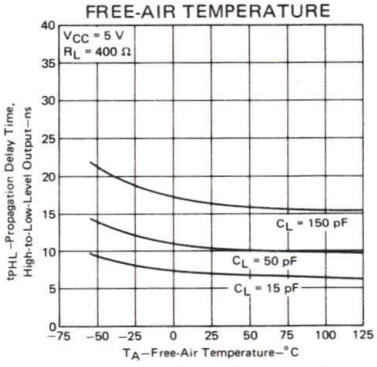


FIGURE A6

† Data for temperatures below 0°C and above 70°C are applicable for Series 54 circuits only.
§ Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

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TYPICAL CHARACTERISTICS†§

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

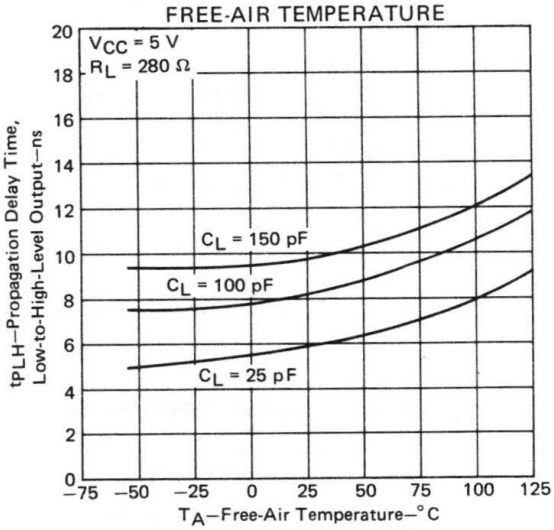

FIGURE B1

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

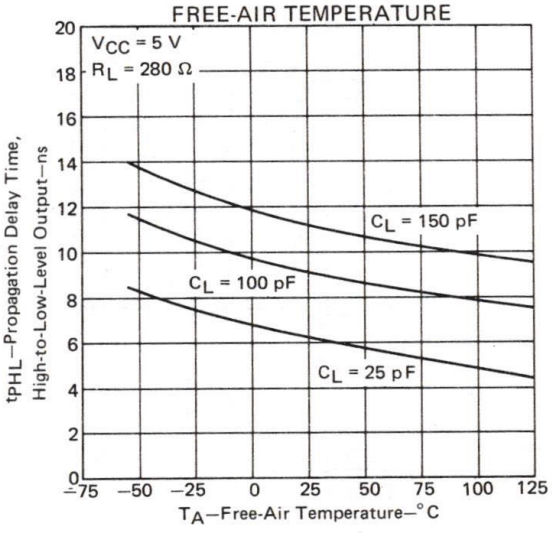

FIGURE B2

AVERAGE PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

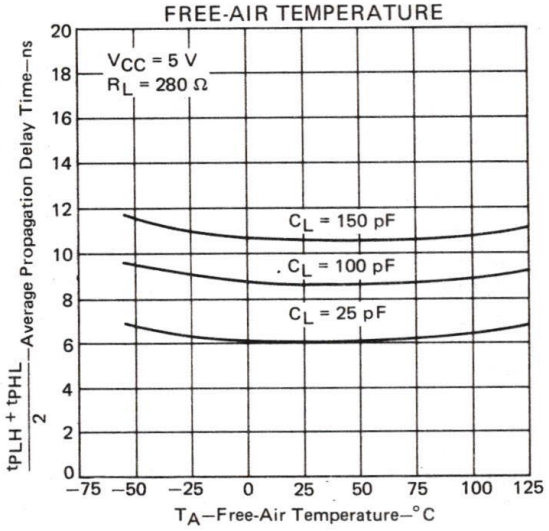

FIGURE B3

†Data for temperatures below 0°C and above 70°C are applicable for Series 54H circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

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TYPICAL CHARACTERISTICS†§

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

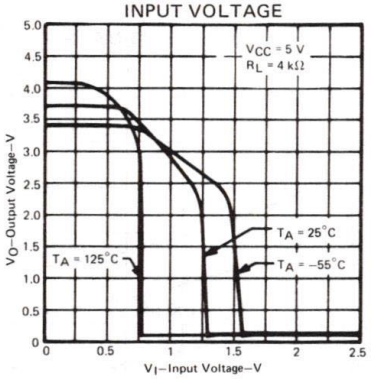

FIGURE C1

OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

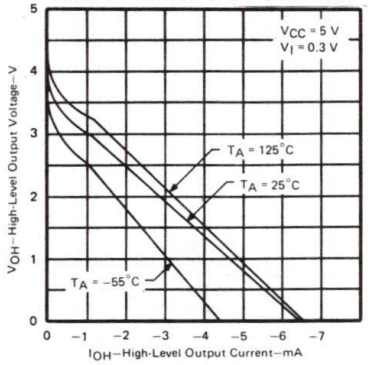

FIGURE C2

OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

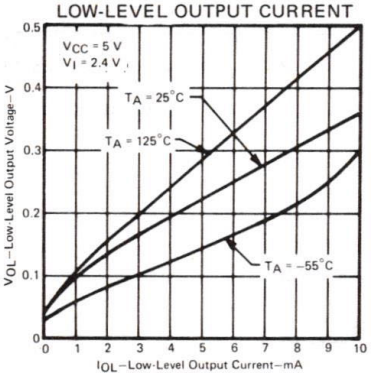

FIGURE C3

CLOCK INPUT CURRENT PER FLIP-FLOP
vs
INPUT VOLTAGE

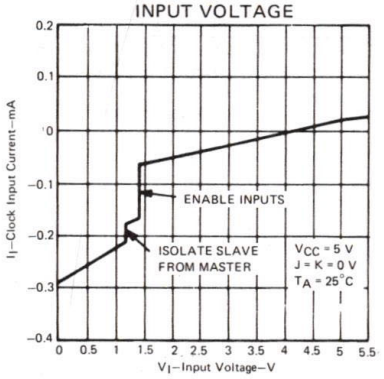

FIGURE C4

POWER DISSIPATION PER FLIP-FLOP
vs
FREQUENCY

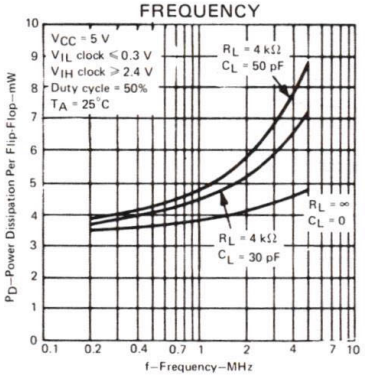

FIGURE C5

AVERAGE TOTAL D-C POWER DISSIPATION
PER FLIP-FLOP
vs
FREE-AIR TEMPERATURE

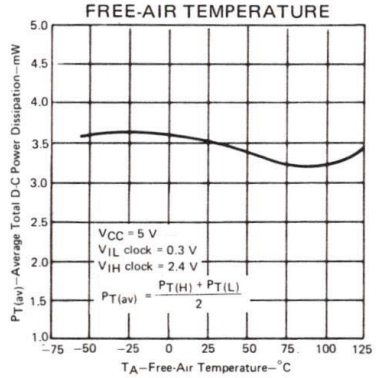

FIGURE C6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54L circuits only.
§Unless otherwise noted, data as shown are applicable specifically for the NAND gates with totem-pole outputs.

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TYPICAL CHARACTERISTICS†§

PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

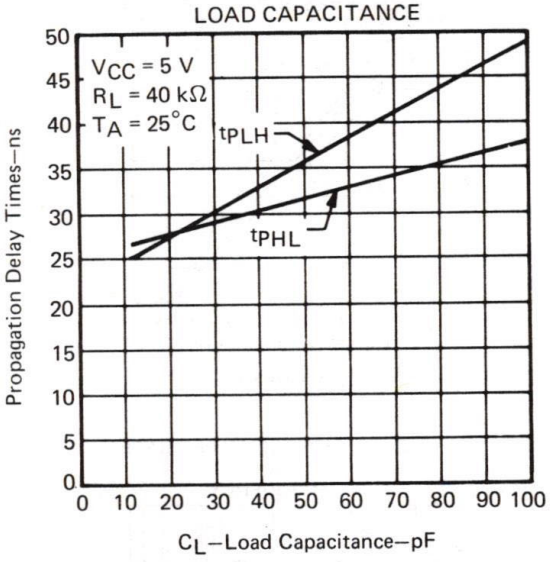

FIGURE C7

AVERAGE PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

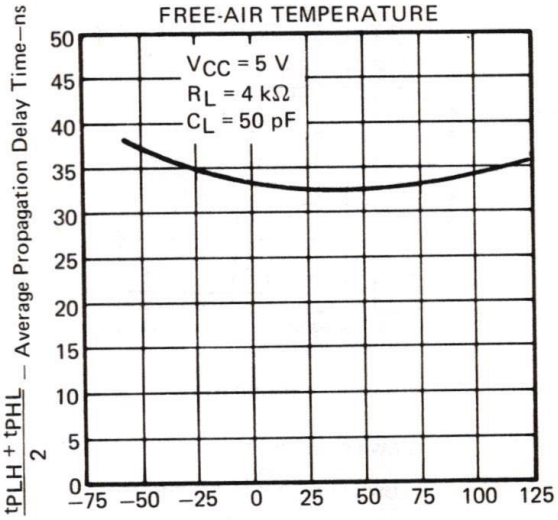

FIGURE C8

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

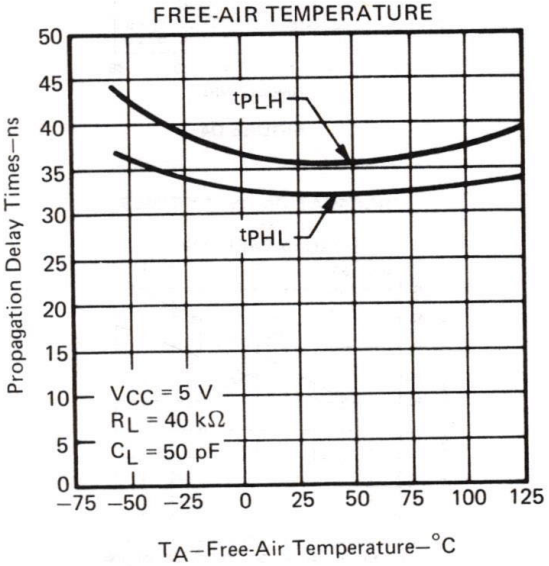

FIGURE C9

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

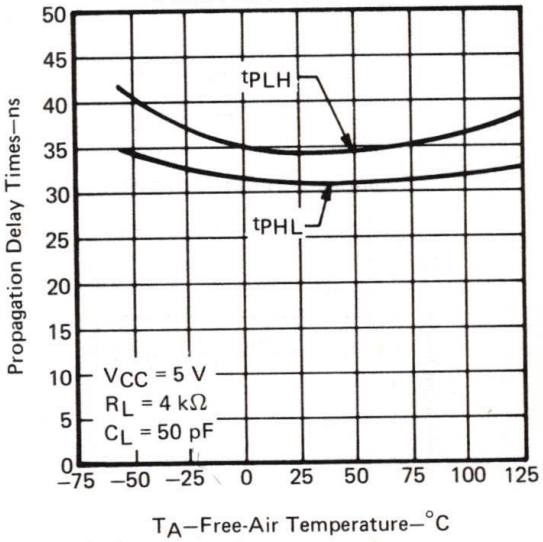

FIGURE C10

† Data for temperatures below 0°C and above 70°C are applicable for Series 54L circuits only.
§ Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†§

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

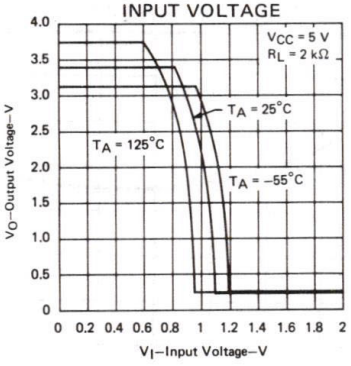

FIGURE D1

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

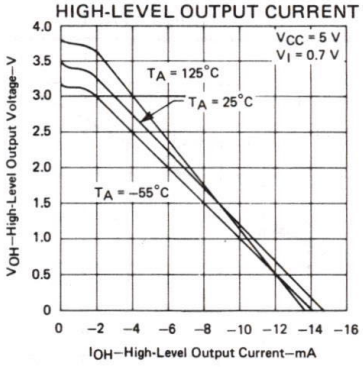

FIGURE D2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

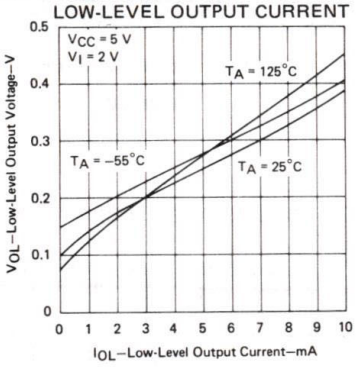

FIGURE D3

POWER DISSIPATION PER GATE
vs
FREQUENCY

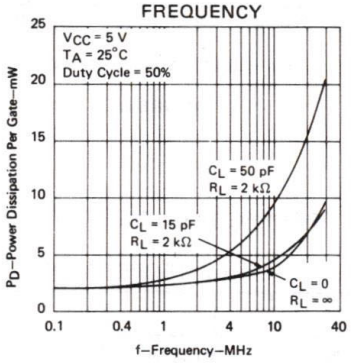

FIGURE D4

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

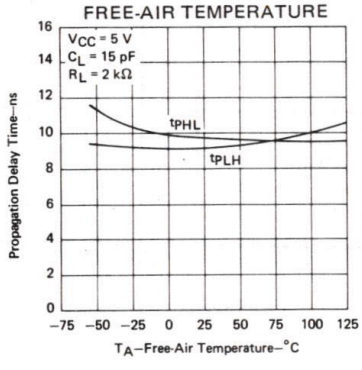

FIGURE D5

PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

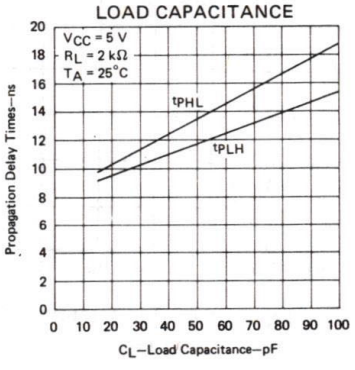

FIGURE D6

† Data for temperatures below 0°C and above 70°C are applicable for Series 54LS circuits only.
§ Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

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TYPICAL CHARACTERISTICS†§

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

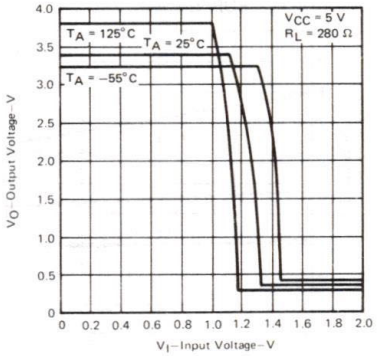

FIGURE E1

INPUT-CLAMPING-DIODE
FORWARD VOLTAGE
vs
FREE-AIR TEMPERATURE

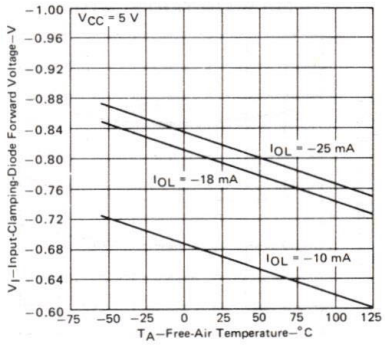

FIGURE E2

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

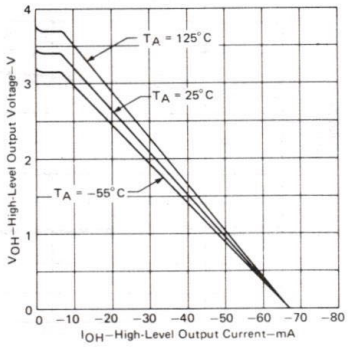

FIGURE E3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

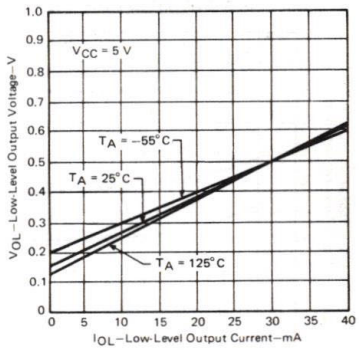

FIGURE E4

INPUT CURRENT
vs
INPUT VOLTAGE

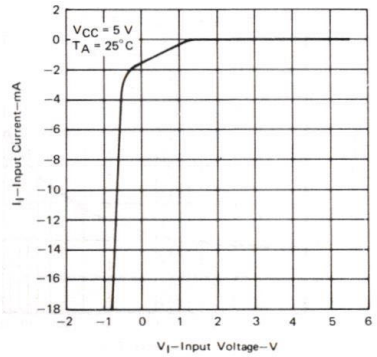

FIGURE E5

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

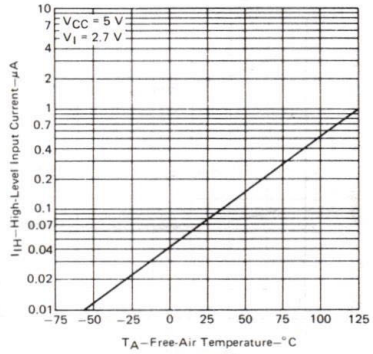

FIGURE E6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

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TYPICAL CHARACTERISTICS†§

PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT vs FREE-AIR TEMPERATURE

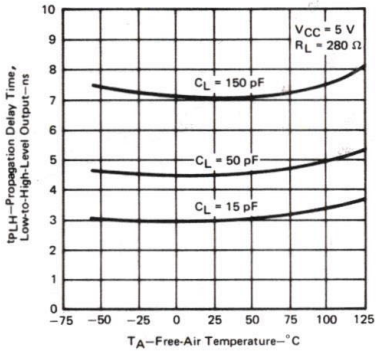

FIGURE E7

PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT vs SUPPLY VOLTAGE

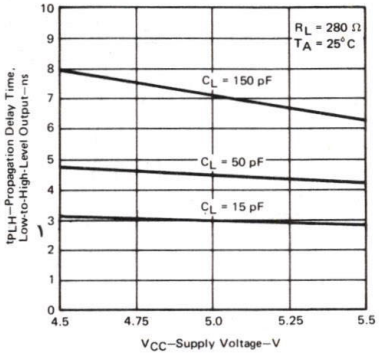

FIGURE E8

PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT vs FREE-AIR TEMPERATURE

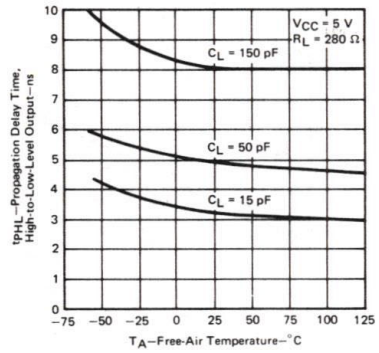

FIGURE E9

PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT vs SUPPLY VOLTAGE

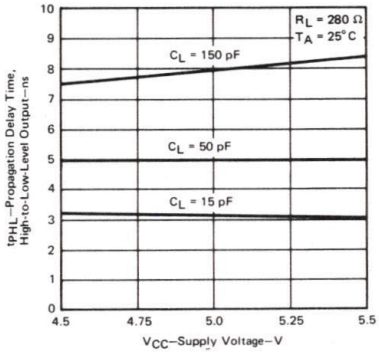

FIGURE E10

AVERAGE PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

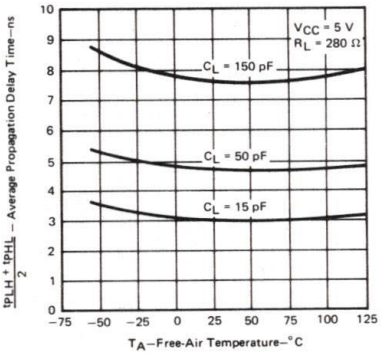

FIGURE E11

POWER DISSIPATION PER GATE vs FREQUENCY

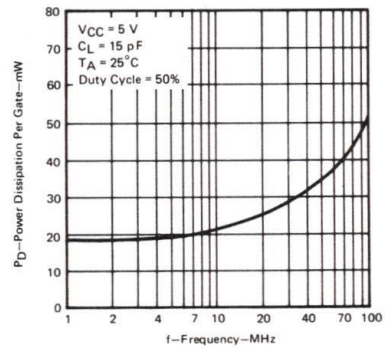

FIGURE E12

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

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TYPICAL CHARACTERISTICS FOR FLIP-FLOPS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

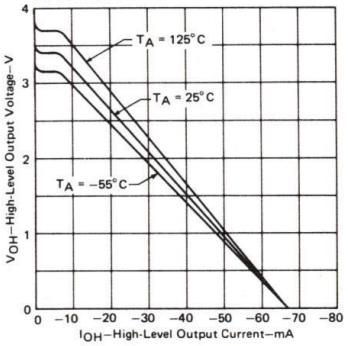

FIGURE E13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

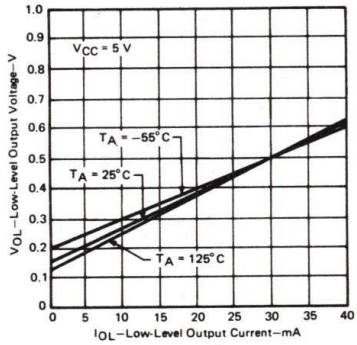

FIGURE E14

'S112, 'S113
INPUT CURRENT
vs
INPUT VOLTAGE

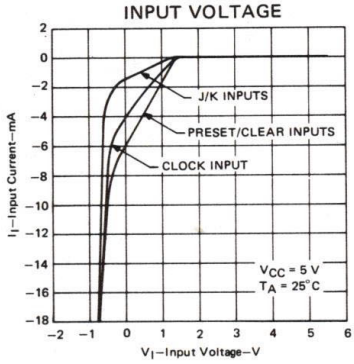

FIGURE E15

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

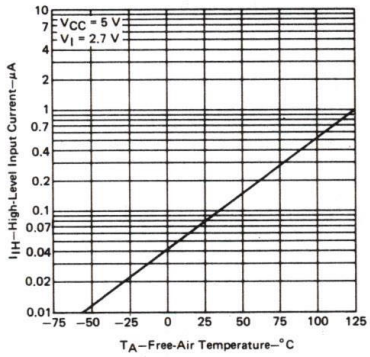

FIGURE E16

'S112, 'S113, 'S114
AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
FREE-AIR TEMPERATURE

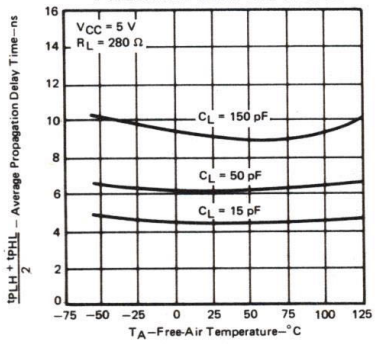

FIGURE E17

'S112, 'S113, 'S114
AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
LOAD CAPACITANCE

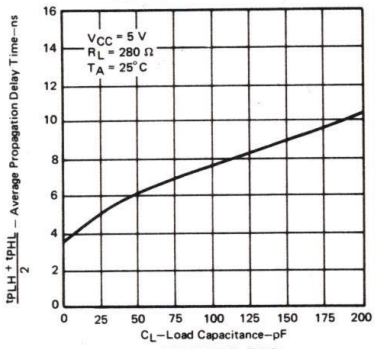

FIGURE E18

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.